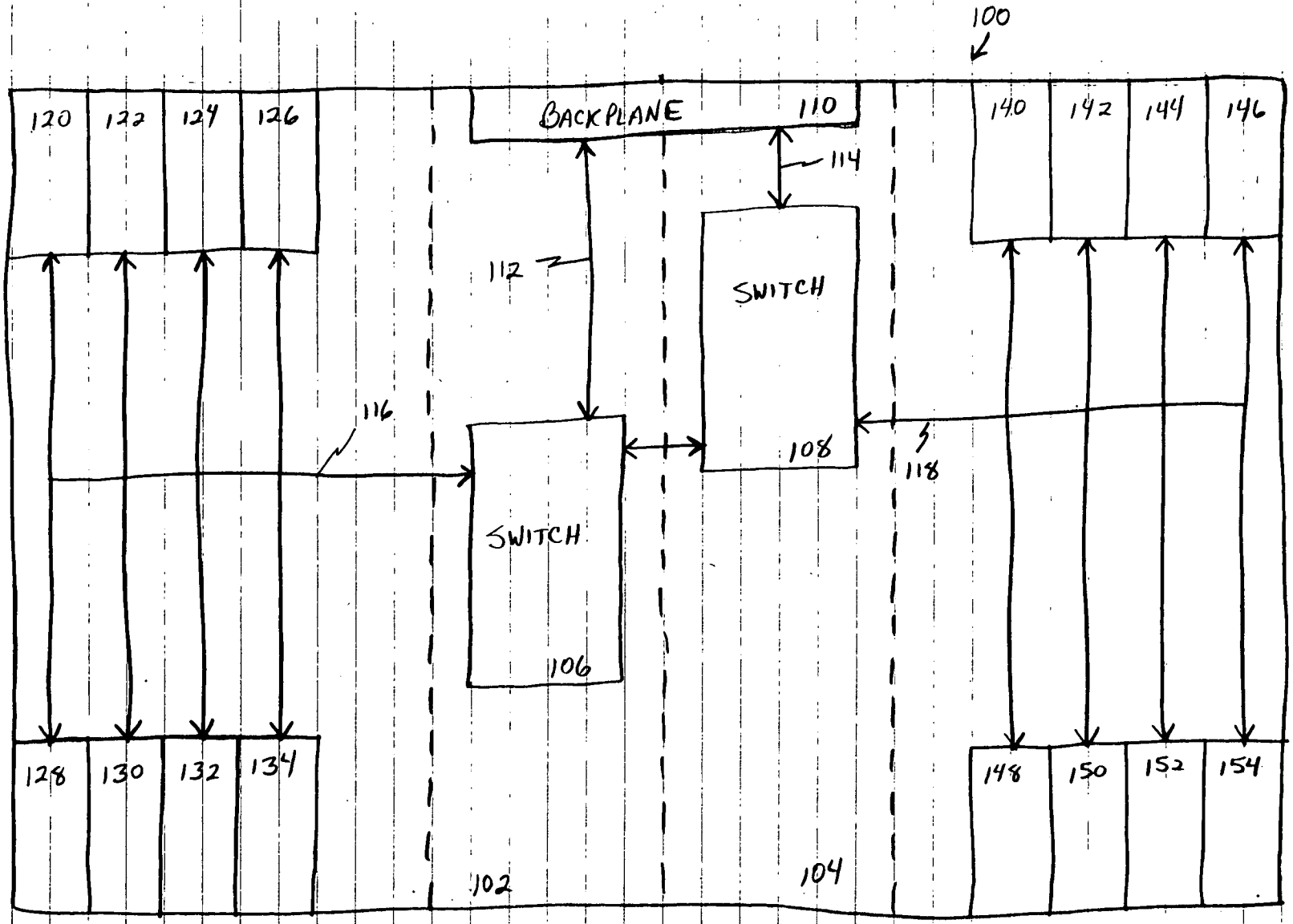
100
BACKPLANE
110
114
112
SWITCH
108
116
118
SWITCH
106
120
122
124
126
128
130
132
134
140
142
144
146
148
150
152
154
102
104

FIGURE 1

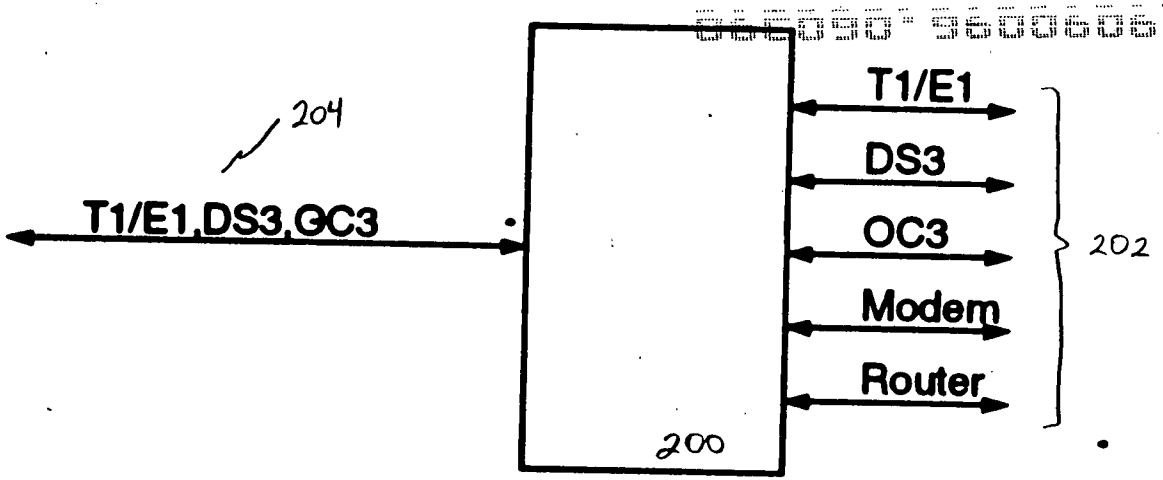

FIGURE 2

86C090 "96006060

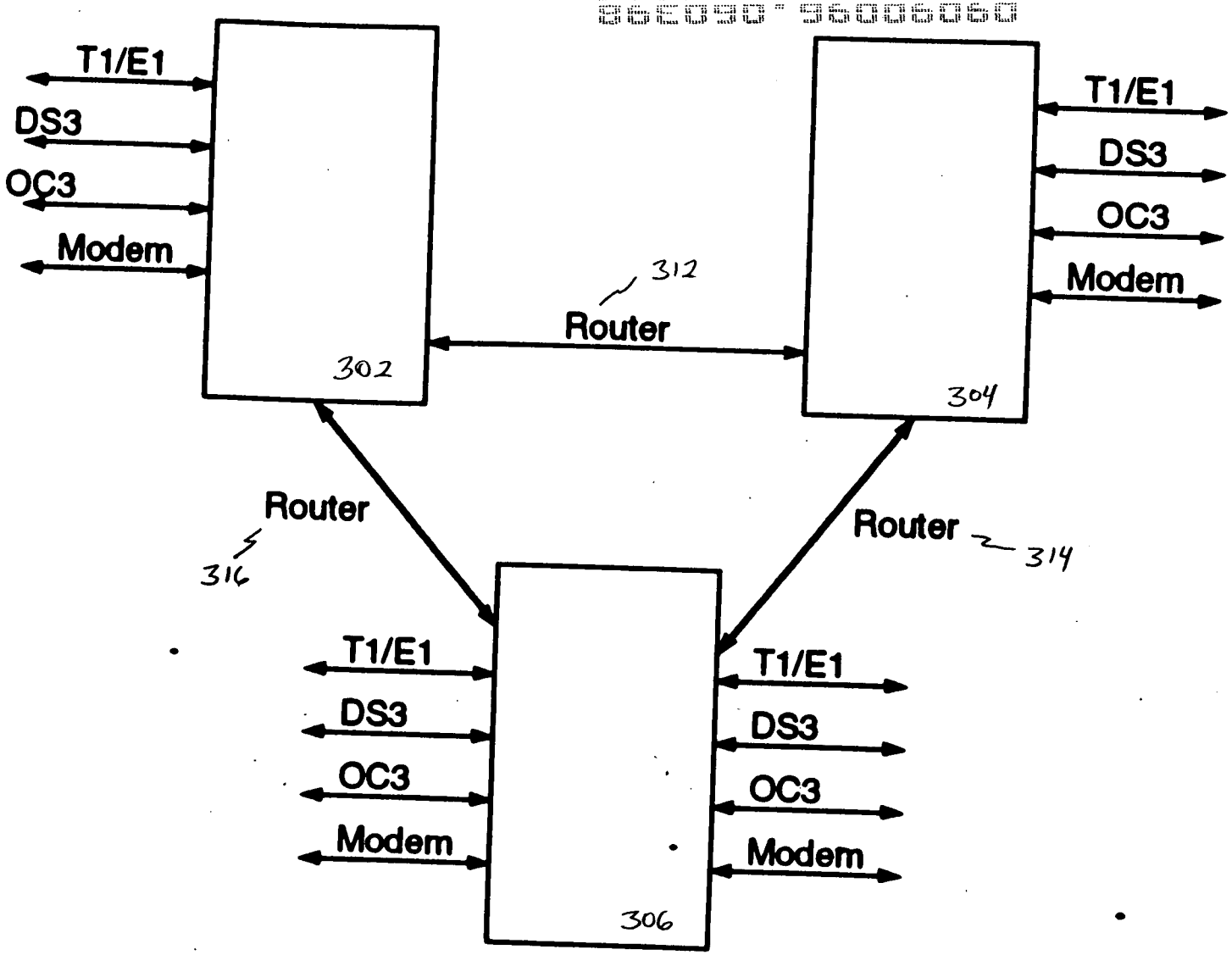

FIGURE 3

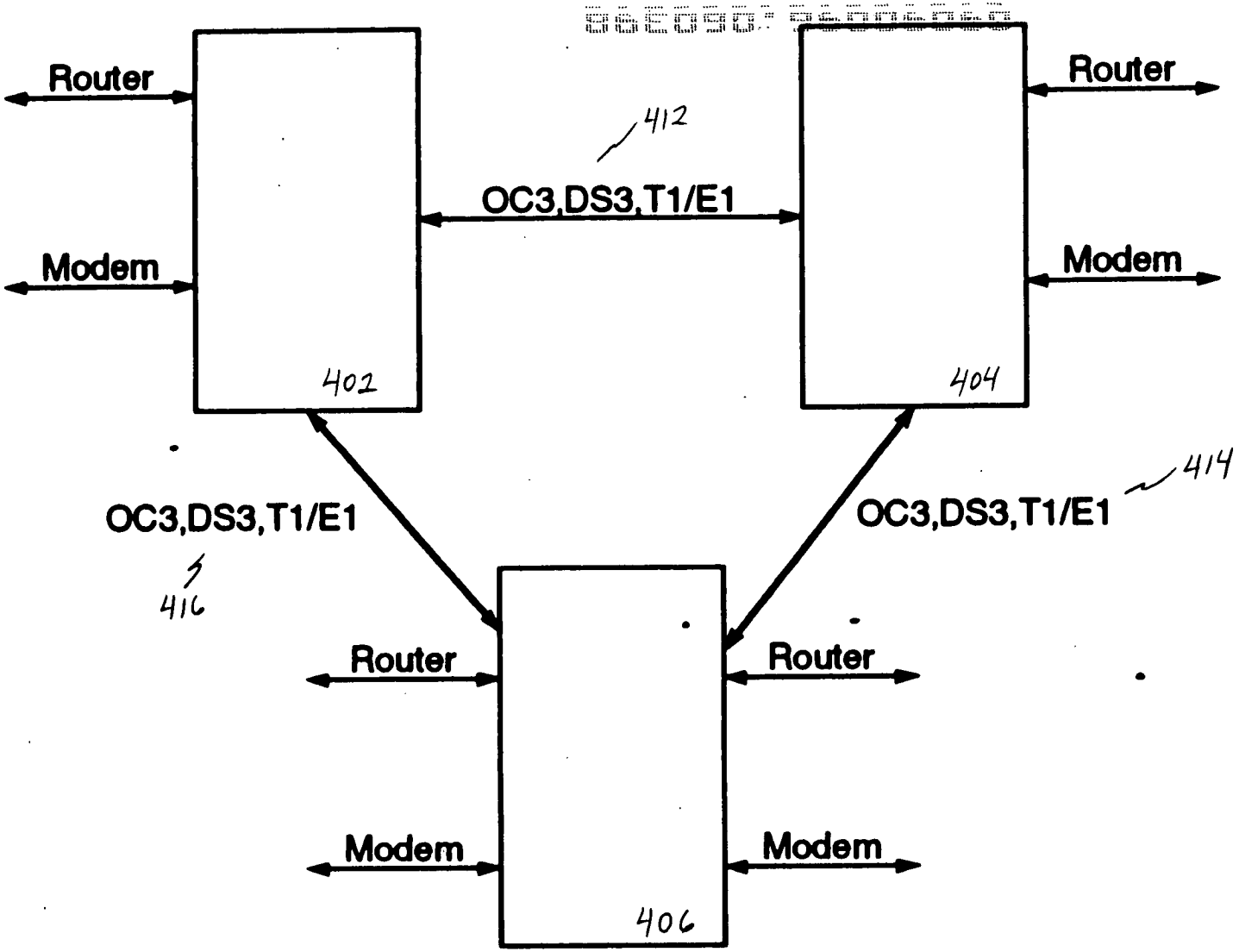
Router
Modem
402
412
OC3,DS3,T1/E1
Router
Modem
404
OC3,DS3,T1/E1
416
OC3,DS3,T1/E1
414
Router
Router
Modem
Modem
406

FIGURE 4

86E090 96006060

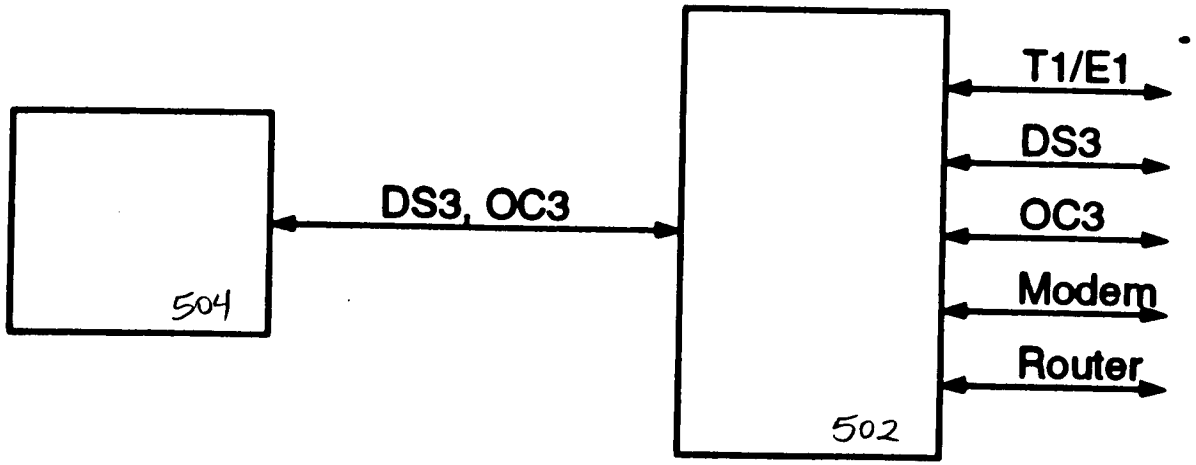

FIGURE 5

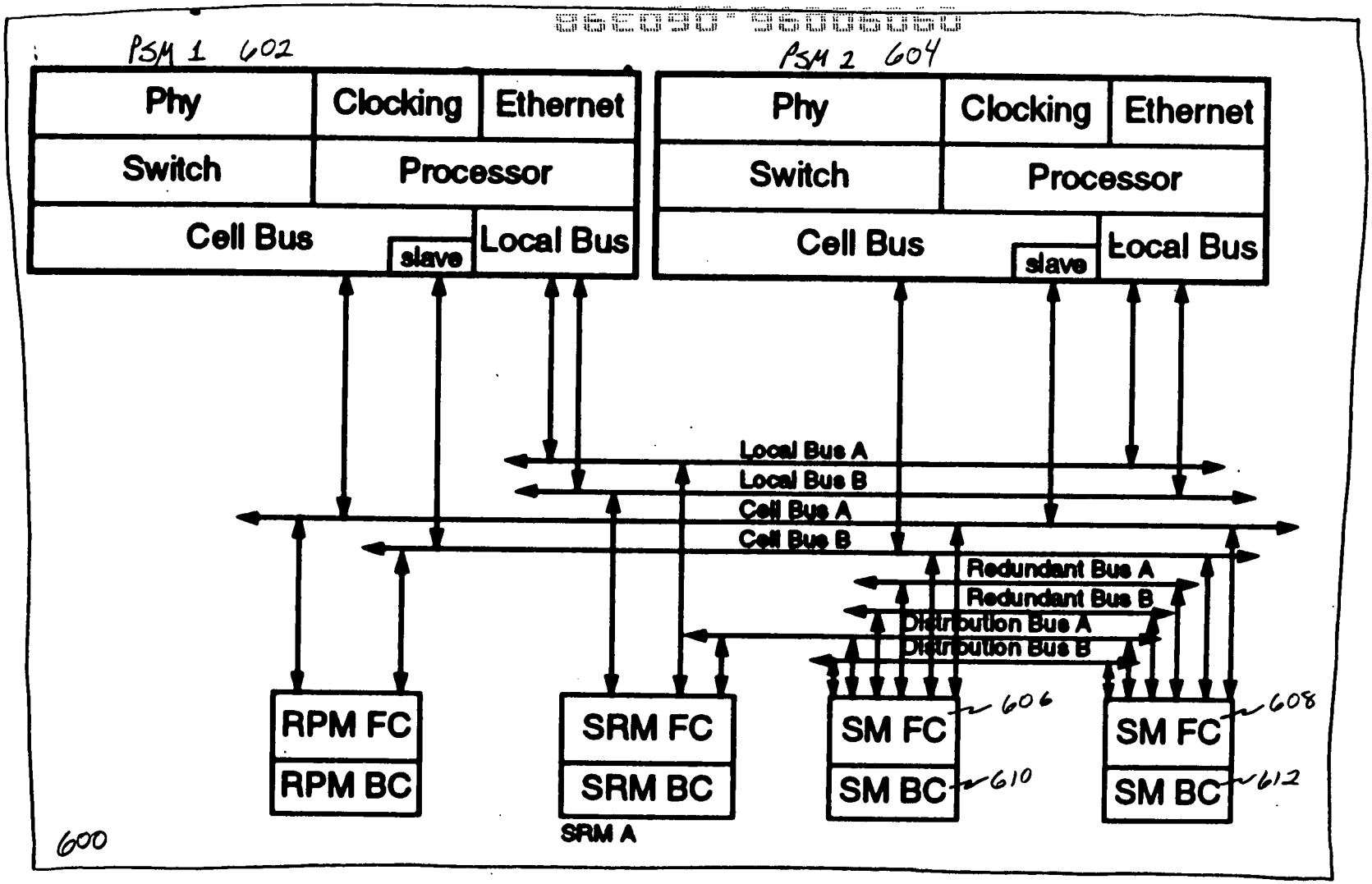
PSM 1 602
PSM 2 604
Phy
Clocking
Ethernet
Switch
Processor
Cell Bus
slave
Local Bus
Local Bus A
Local Bus B
Cell Bus A
Cell Bus B
Redundant Bus A
Redundant Bus B
Distribution Bus A
Distribution Bus B
RPM FC
RPM BC
SRM FC
SRM BC
SRM A
SM FC
SM BC
606
610
608
612
600

FIGURE 6

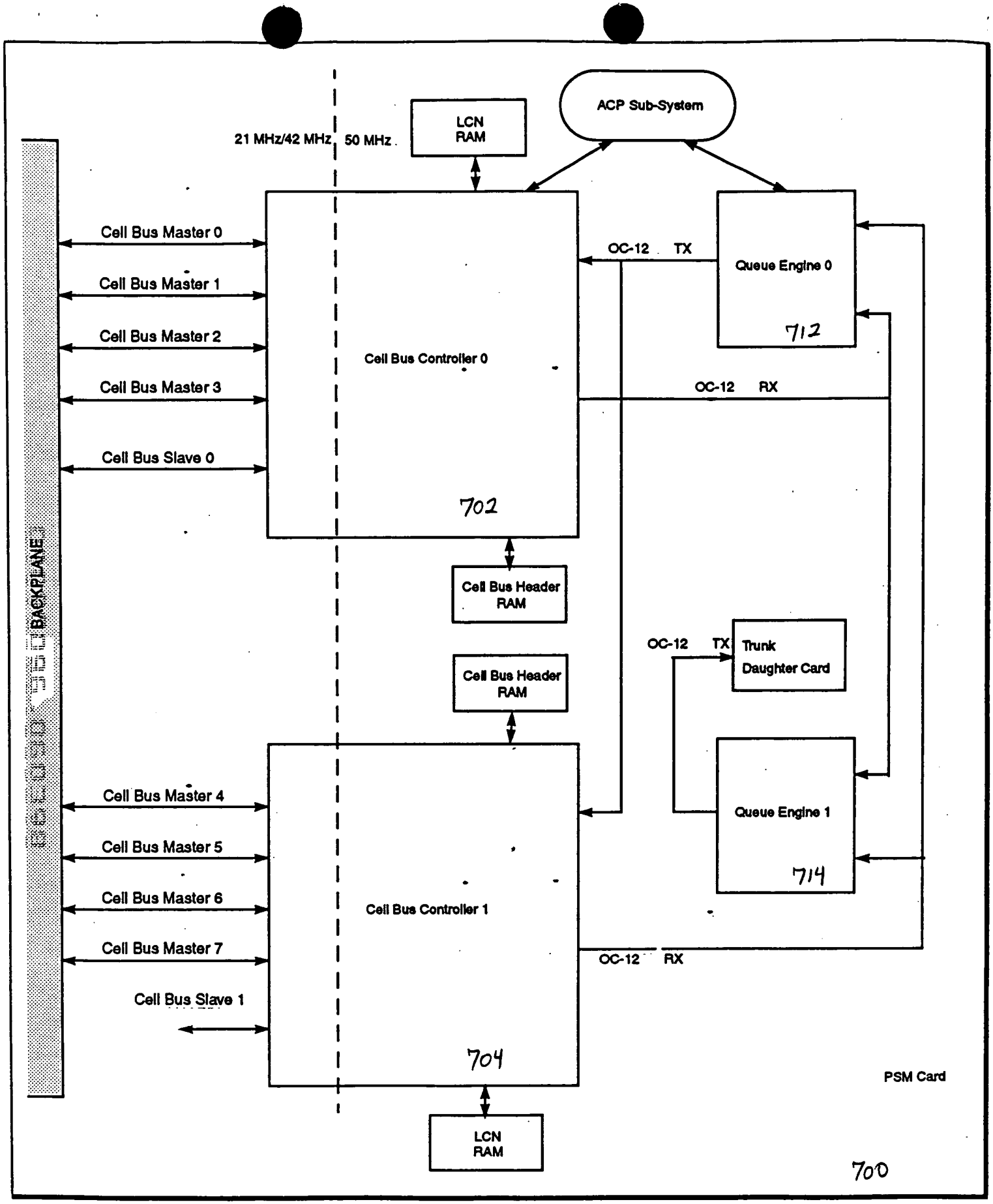
ACP Sub-System
LCN RAM
21 MHz/42 MHz
50 MHz
Cell Bus Master 0
Cell Bus Master 1
Cell Bus Master 2
Cell Bus Master 3
Cell Bus Slave 0
Cell Bus Controller 0
702
OC-12 TX
Queue Engine 0
712
OC-12 RX
Cell Bus Header RAM
Cell Bus Header RAM
OC-12 TX
Trunk Daughter Card
Queue Engine 1
714
Cell Bus Master 4
Cell Bus Master 5
Cell Bus Master 6
Cell Bus Master 7
Cell Bus Slave 1
Cell Bus Controller 1
704
OC-12 RX
PSM Card
LCN RAM
700
BACKPLANE

FIGURE 7

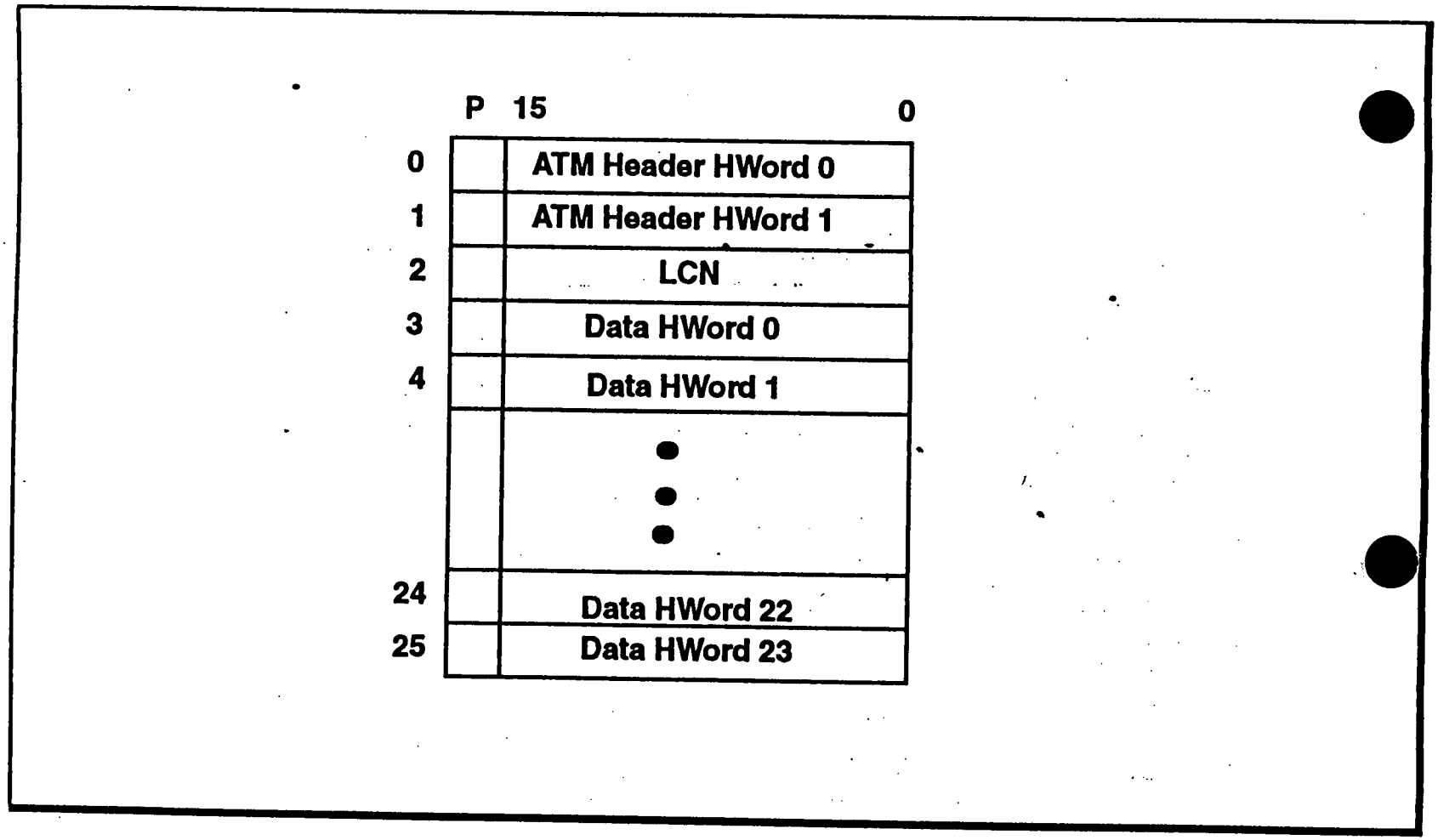
P 15 0
0
ATM Header HWord 0
1
ATM Header HWord 1
2
LCN
3
Data HWord 0
4
Data HWord 1
24
Data HWord 22
25
Data HWord 23

FIGURE 8

86050 3606060

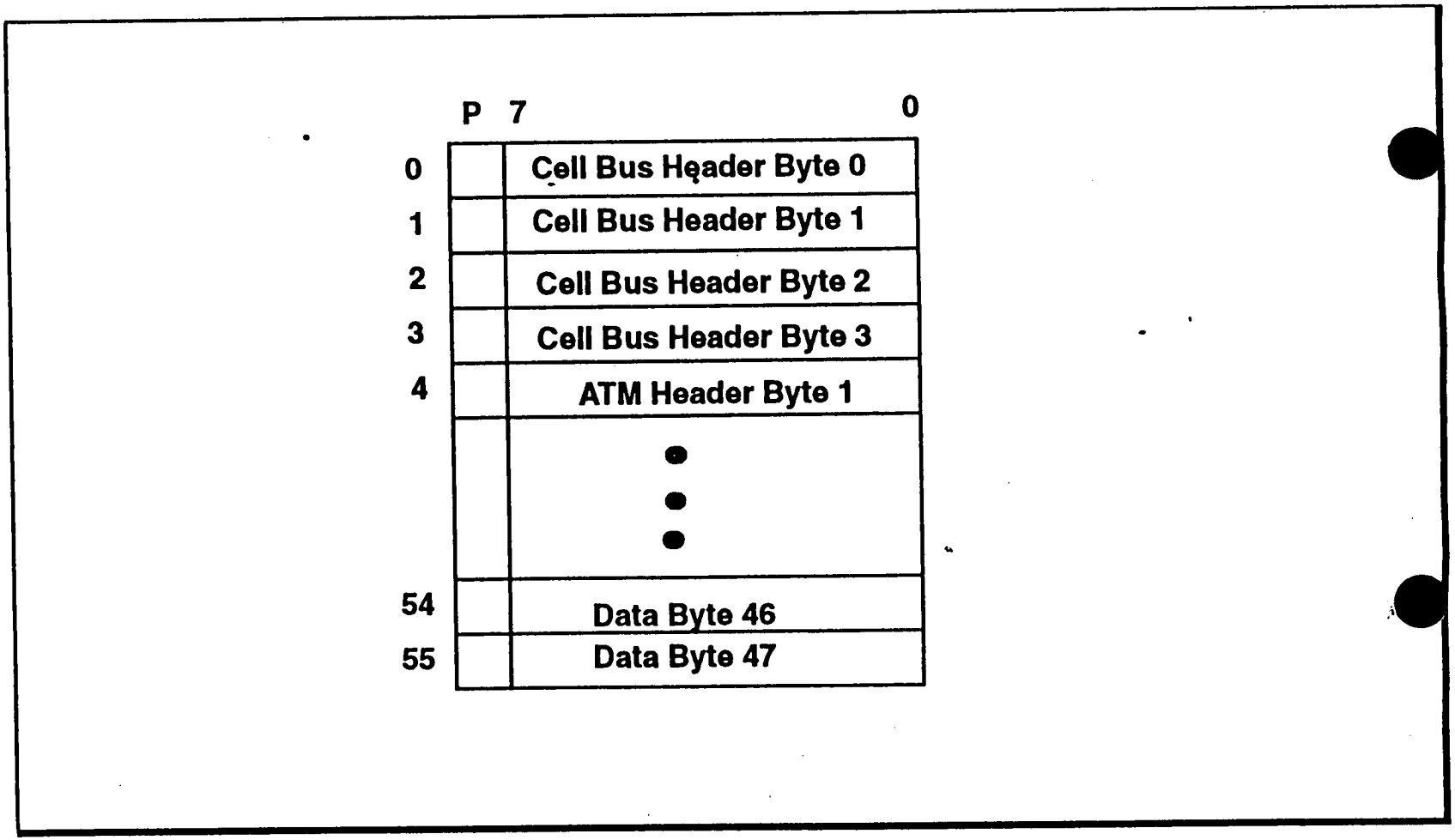

FIGURE 9

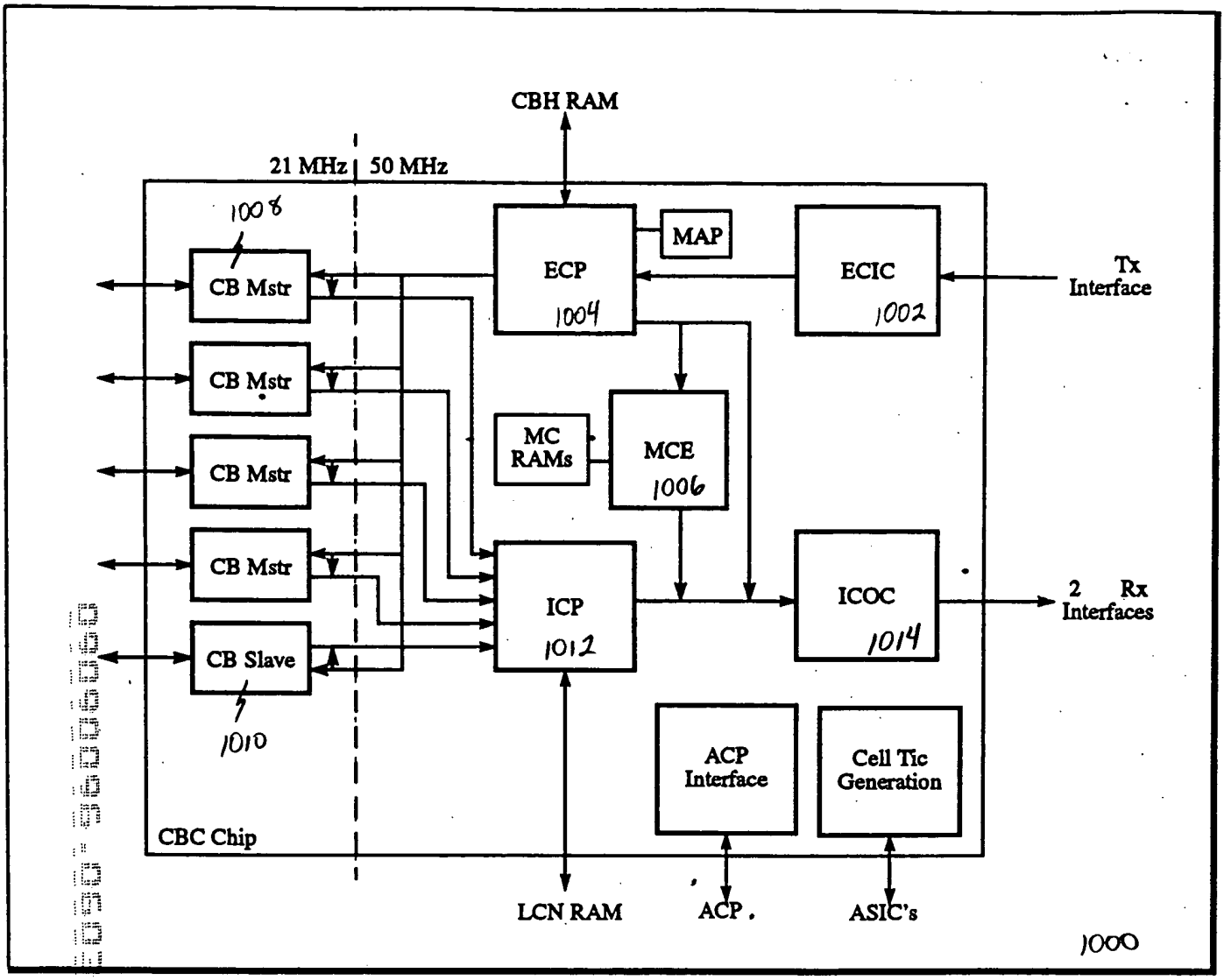
CBH RAM
21 MHz
50 MHz
1008
CB Mstr
CB Mstr
CB Mstr
CB Mstr
CB Slave
1010
ECP
1004
MAP
ECIC
1002
Tx
Interface
MC
RAMs
MCE
1006
ICP
1012
ICOC
1014
2 Rx
Interfaces
ACP
Interface
Cell Tic
Generation
CBC Chip
LCN RAM
ACP
ASIC's
1000

FIGURE 10

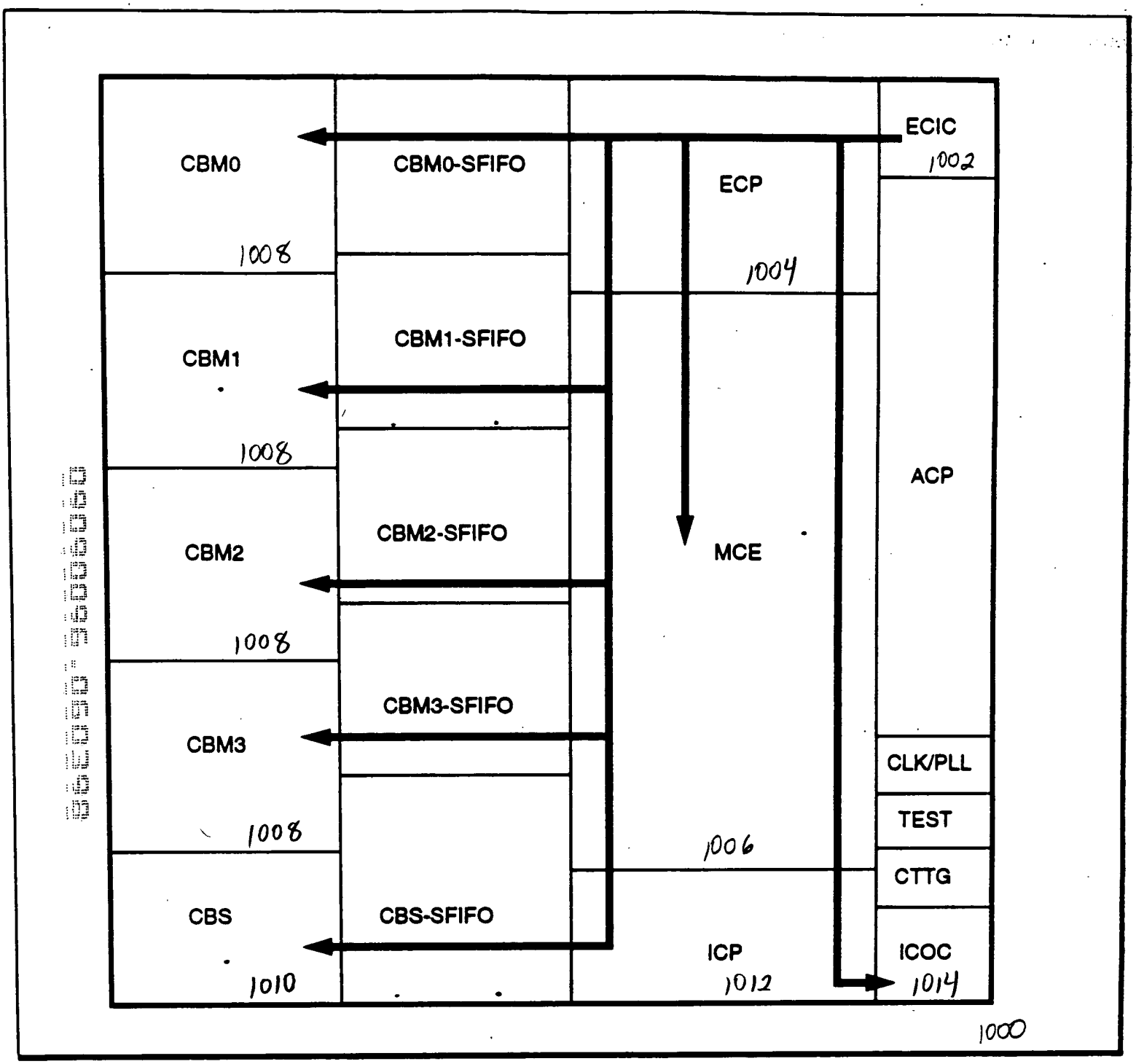
CBM0
CBM0-SFIFO
ECIC
1002
ECP
1008
1004
CBM1
CBM1-SFIFO
1008
ACP
CBM2
CBM2-SFIFO
MCE
1008
CBM3
CBM3-SFIFO
CLK/PLL
TEST
1008
1006
CBS
CBS-SFIFO
CTTG
ICP
ICOC
1010
1012
1014
1000

FIGURE 11

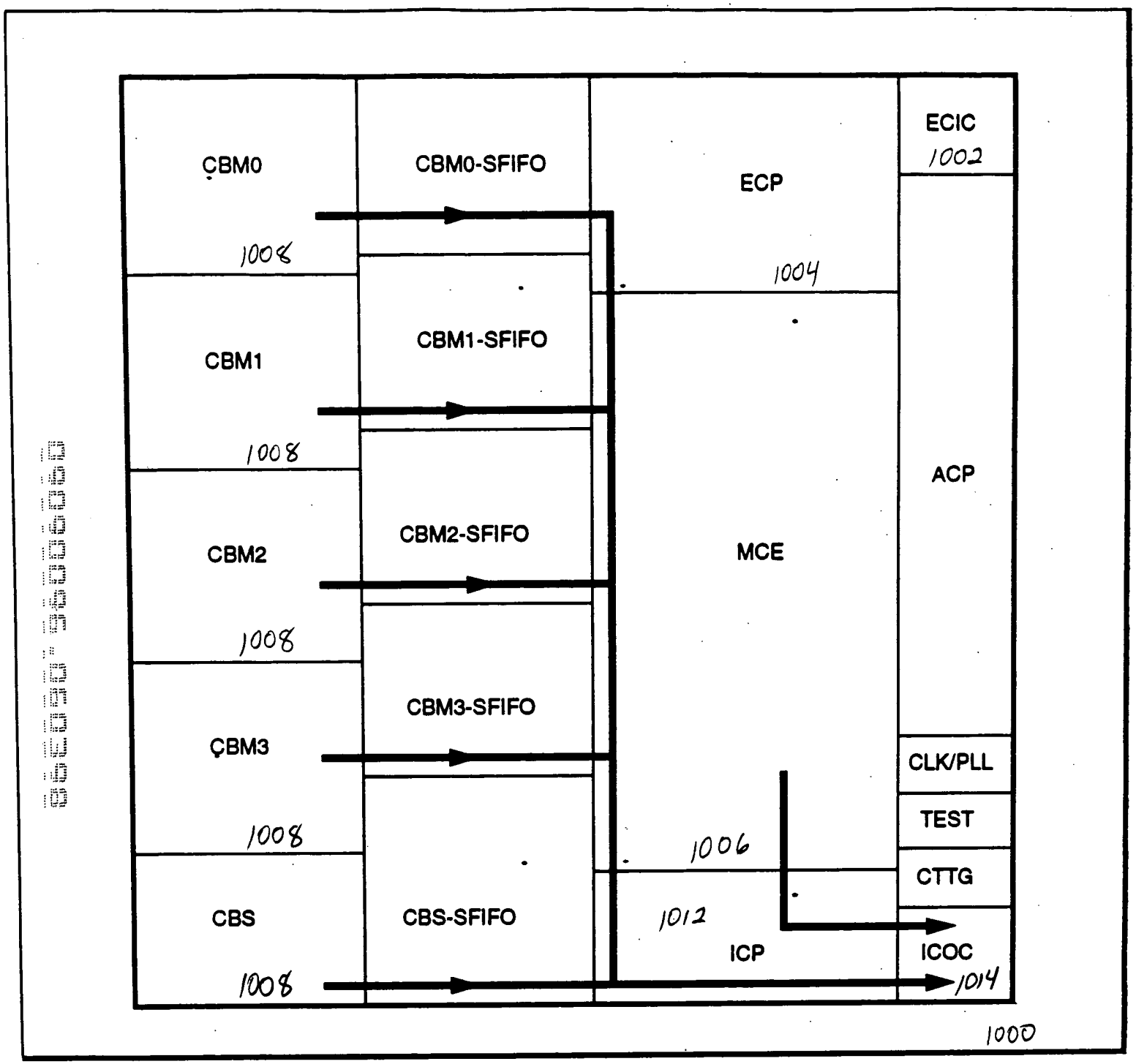
CBM0
CBM0-SFIFO
ECP
ECIC
1002
1008
1004
CBM1
CBM1-SFIFO
1008
ACP
CBM2
CBM2-SFIFO
MCE
1008
CBM3-SFIFO
CBM3
CLK/PLL
TEST
1008
1006
CTTG
CBS
CBS-SFIFO
1012
ICP
ICOC
1008
1014
1000

FIGURE 12

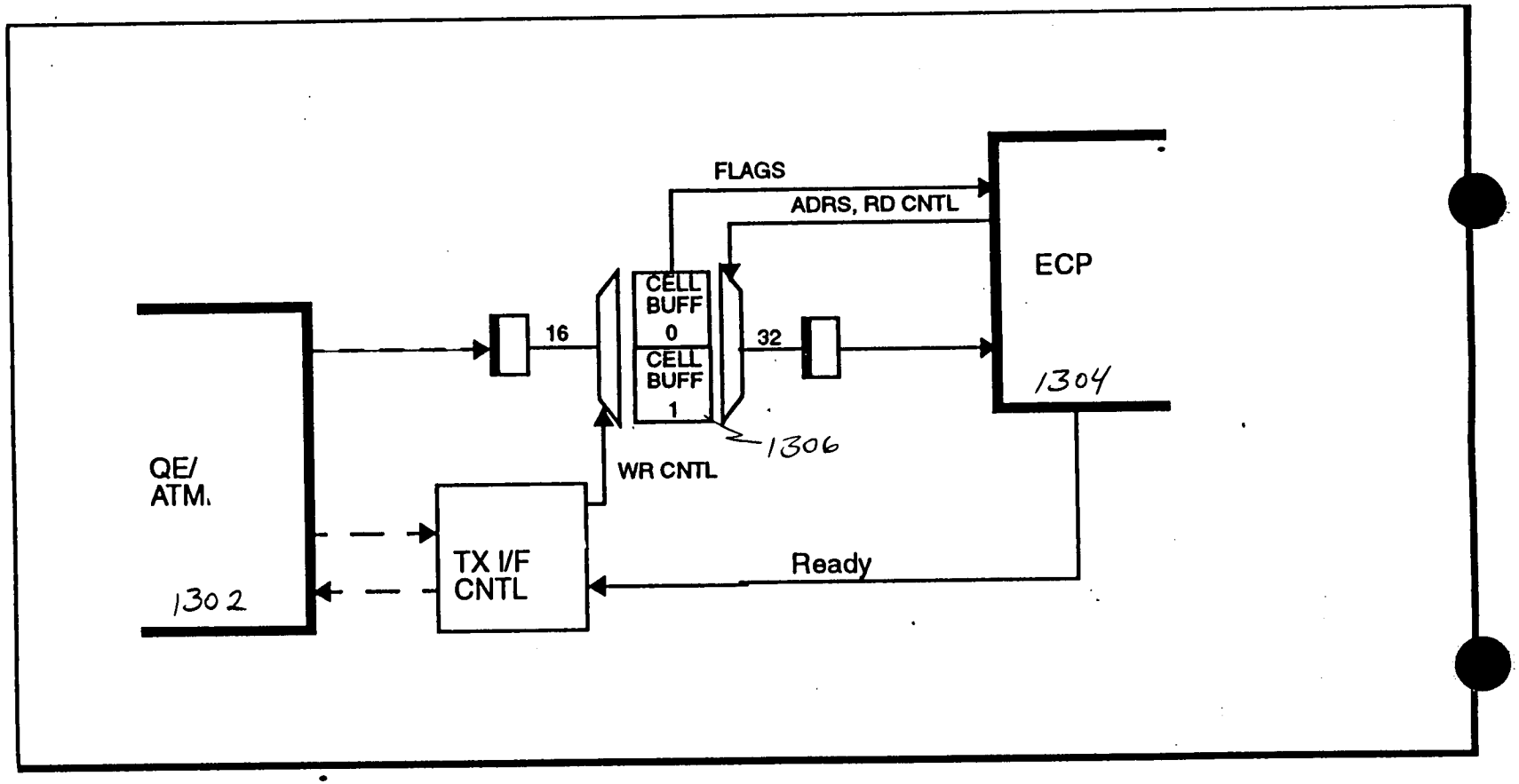
FLAGS
ADRS, RD CNTL
ECP
CELL BUFF 0
CELL BUFF 1
16
32
1304
1306
WR CNTL
QE/ ATM.
1302
TX I/F CNTL
Ready

FIGURE 13

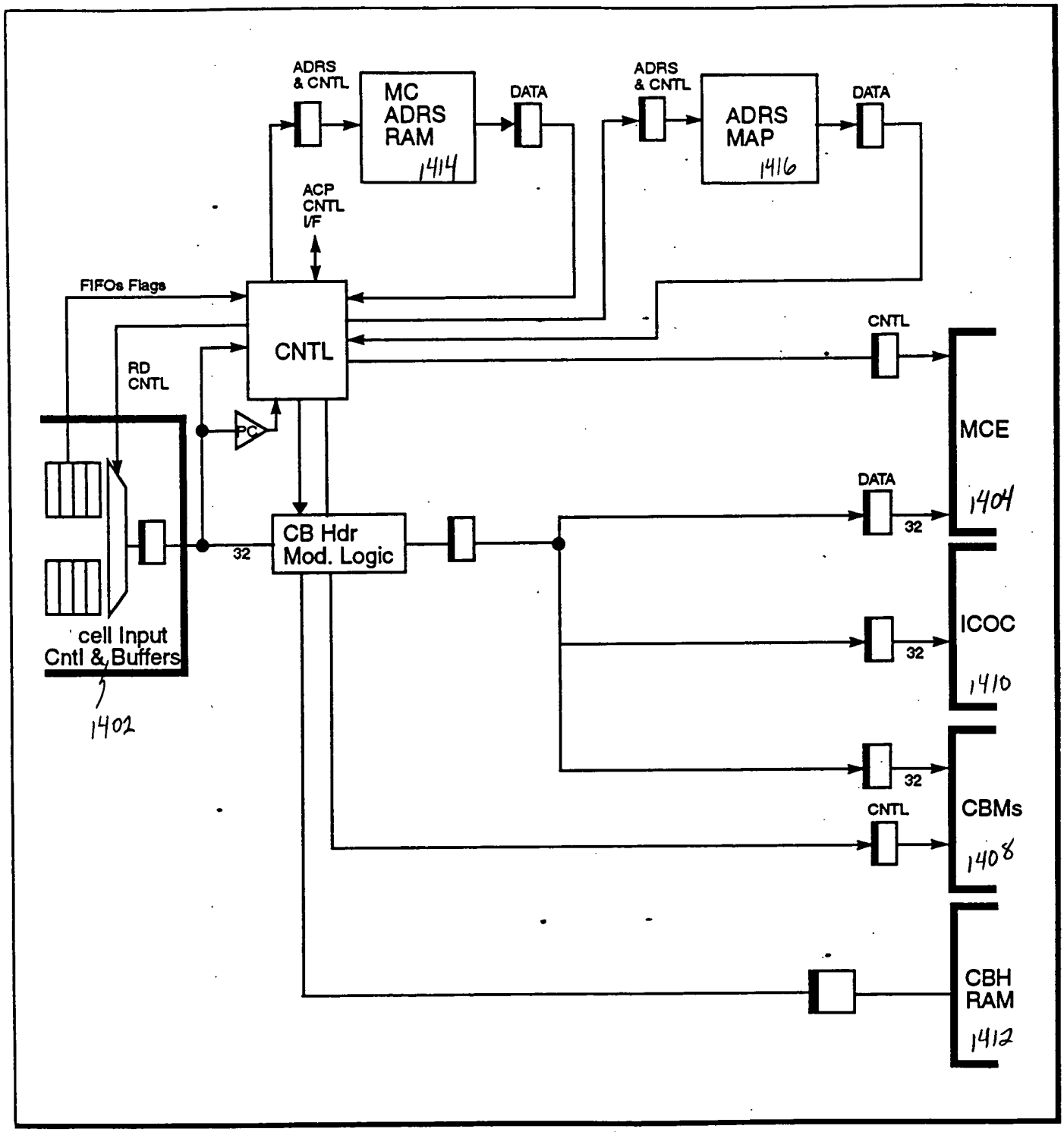
ADRS & CNTL
MC ADRS RAM
1414
DATA
ADRS & CNTL
ADRS MAP
1416
DATA
ACP CNTL I/F
FIFOs Flags
CNTL
RD CNTL
CNTL
MCE
1404
PC
DATA
32
CB Hdr Mod. Logic
32
ICOC
1410
32
CBMs
1408
CNTL
cell Input Cntl & Buffers
1402
CBH RAM
1412

FIGURE 14

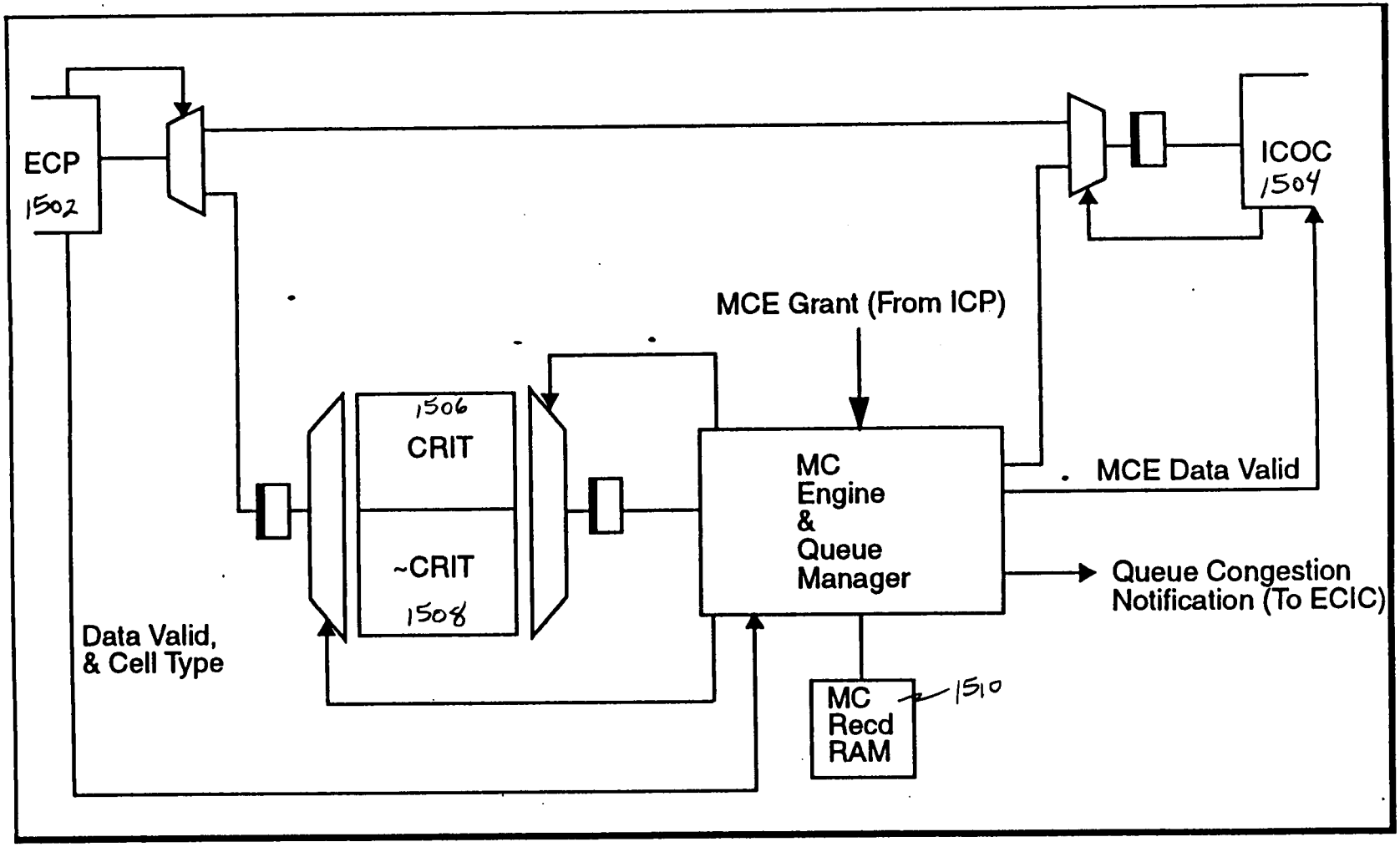
ECP
1502
ICOC
1504
MCE Grant (From ICP)
1506
CRIT
~CRIT
1508
MC
Engine
&
Queue
Manager
MCE Data Valid
Queue Congestion
Notification (To ECIC)
Data Valid,
& Cell Type
MC
Recd
RAM
1510

FIGURE 15

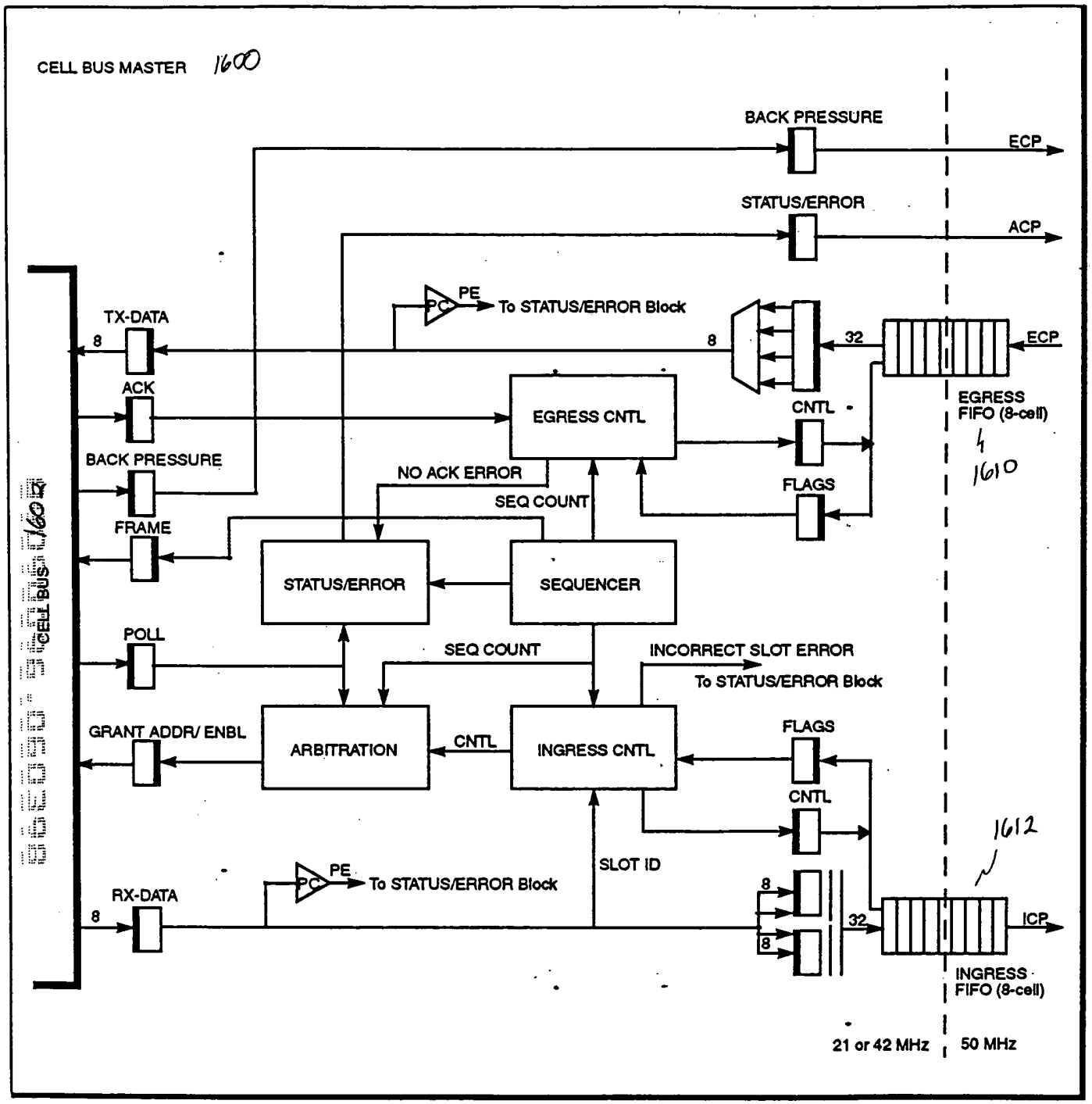
CELL BUS MASTER 1600
BACK PRESSURE
ECP
STATUS/ERROR
ACP
PE
PC
To STATUS/ERROR Block
TX-DATA
8
8
32
ECP
ACK
EGRESS CNTL
CNTL
EGRESS FIFO (8-cell)
1610
BACK PRESSURE
NO ACK ERROR
SEQ COUNT
FLAGS
FRAME
STATUS/ERROR
SEQUENCER
POLL
SEQ COUNT
INCORRECT SLOT ERROR
To STATUS/ERROR Block
GRANT ADDR/ ENBL
ARBITRATION
CNTL
INGRESS CNTL
FLAGS
CNTL
1612
SLOT ID
PE
PC
To STATUS/ERROR Block
RX-DATA
8
8
8
32
ICP
INGRESS FIFO (8-cell)
21 or 42 MHz
50 MHz
CELL BUS 1602

FIGURE 16

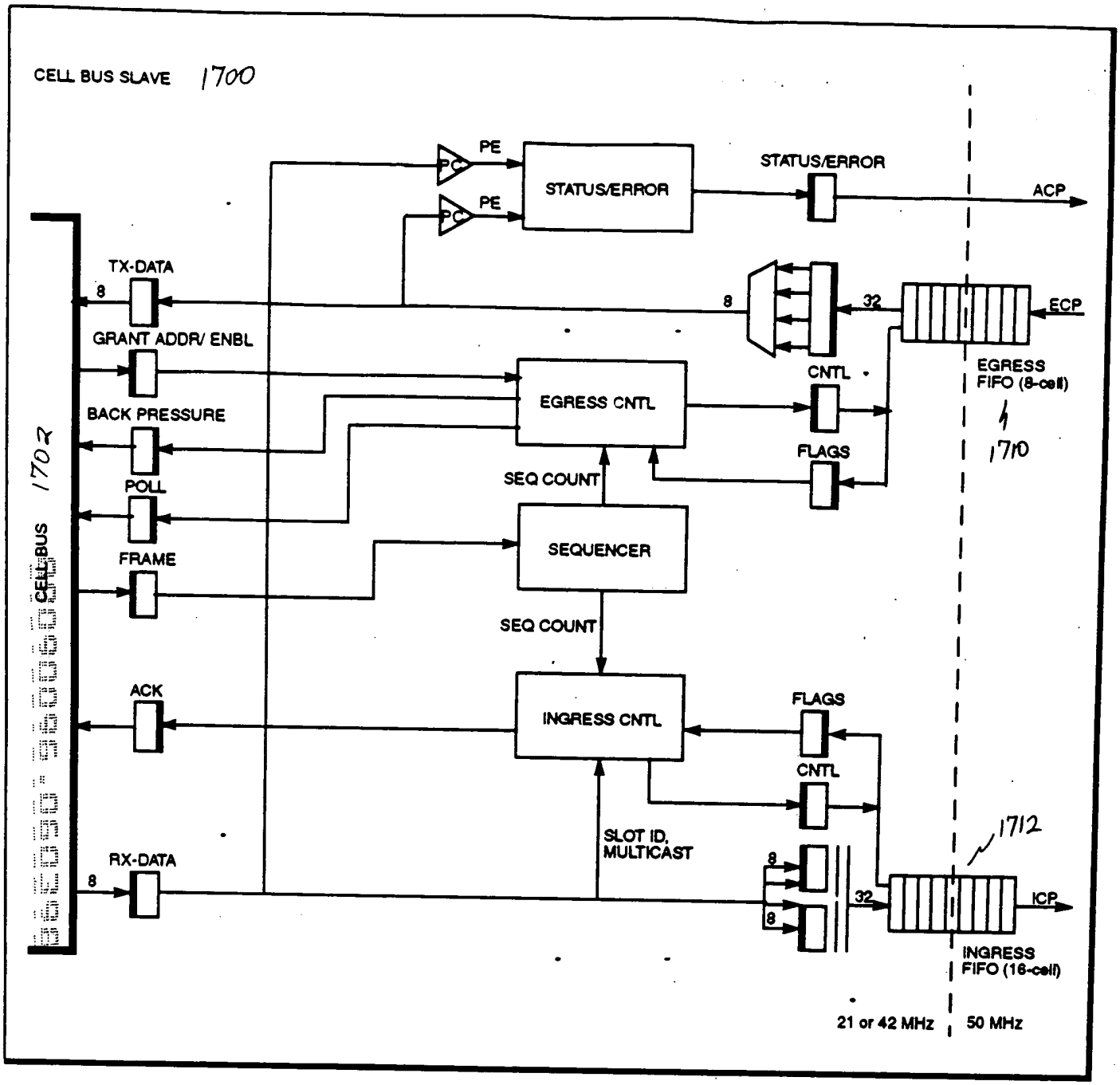
CELL BUS SLAVE 1700
PE
PE
STATUS/ERROR
STATUS/ERROR
ACP
TX-DATA
8
8
32
ECP
GRANT ADDR/ ENBL
EGRESS CNTL
CNTL
EGRESS FIFO (8-cell)
1710
BACK PRESSURE
FLAGS
SEQ COUNT
POLL
SEQUENCER
FRAME
SEQ COUNT
CELL BUS 1702
ACK
INGRESS CNTL
FLAGS
CNTL
1712
SLOT ID, MULTICAST
RX-DATA
8
8
8
32
ICP
INGRESS FIFO (16-cell)
21 or 42 MHz
50 MHz

FIGURE 17

Cell Bus Cycle	Tx Frame	Poll	Grant Address	Grant Enable	Reset	Tx Data (To Slave)	Rx Data (From Slave)	Ack_Lo
0/58	1	0	0	1	0	First Byte of Cell	0	1
1	0			0			First Byte	
2		Odd Request				Byte 2	Byte 2	
3		0				Byte 3	Byte 3	
4						Byte 4	Byte 4	
5						Byte 5	Byte 5	
6-9						Bytes 6-9	Bytes 6-9	0 (CBM checks at Cycle 18 only)
10		Even Request				Byte 10	Byte 10	
11-14		0				Bytes 11-14	Bytes 11-14	
15			Slot to Reset	Reset Type	1	Byte 15	Byte 15	
16						Byte 16	Byte 16	
17						Byte 17	Byte 17	
18		Odd Ready	0	0	0	Byte 18	Byte 18	
19-25		0				Bytes 19-25	Bytes 19-25	
26		Even Ready				Byte 26	Byte 26	
27-33		0				Bytes 27-33	Bytes 27-33	
34		Odd Present				Byte 34	Byte 34	
35-41		0				Bytes 35-41	Bytes 35-41	
42		Even Present				Byte 42	Byte 42	
43-49		0				Bytes 43-49	Bytes 43-49	
50		Odd Stop				Byte 50	Byte 50	
51		0	Grant	1		Byte 51	Byte 51	
52			0			Byte 52	Byte 52	
53						Byte 53	Byte 53	
54						Byte 54	Byte 54	
55						Byte 55	Byte 55	
56		Even Stop				Byte 56	Byte 56	
57		0				0	0	
58/0	1					First Byte of next cell		1

FIGURE 18

Cell Bus Cycle	Tx Frame	Poll	Grant Address	Grant Enable	Reset	Tx Data (From CBM)	Rx Data (To CBM)	Ack_Lo
0/58	1	Hi-Z		1		First Byte of Cell	Hi-Z	0
1		Odd Request					First Byte	
2						Byte 2	Byte 2	Hi-Z
3						Byte 3	Byte 3	
4						Byte 4	Byte 4	
5		Hi-Z	0			Byte 5	Byte 5	
6-8				0	0	Bytes 6-8	Bytes 6-8	
9		Even Request				Byte 9	Byte 9	
10						Byte 10	Byte 10	
11						Byte 11	Byte 11	
12-14		Hi-Z				Bytes 12-14	Bytes 12-14	
15			Slot to Reset			Byte 15	Byte 15	
16				Reset Type		Byte 16	Byte 16	
17		Odd Ready			1	Byte 17	Byte 17	
18						Byte 18	Byte 18	
19						Byte 19	Byte 19	
20-24		Hi-Z				Bytes 20-24	Bytes 20-24	
25		Even Ready				Byte 25	Byte 25	
26						Byte 26	Byte 26	
27	0					Byte 27	Byte 27	
27-32		Hi-Z				Bytes 27-32	Bytes 27-32	
33		Odd Present				Byte 33	Byte 33	
34			0	0		Byte 34	Byte 34	0
35						Byte 35	Byte 35	
35-40		Hi-Z				Bytes 35-40	Bytes 35-40	
41		Even Present				Byte 41	Byte 41	
42						Byte 42	Byte 42	
43					0	Byte 43	Byte 43	
43-48		Hi-Z				Bytes 43-48	Bytes 43-48	
49		Odd Stop				Byte 49	Byte 49	
50						Byte 50	Byte 50	
51			Grant			Byte 51	Byte 51	
52		Hi-Z				Byte 52	Byte 52	
53						Byte 53	Byte 53	
54						Byte 54	Byte 54	
55		Even Stop	0	1		Byte 55	Byte 55	
56						Byte 56	Byte 56	
57						0	Hi-Z	
58/0	1	Hi-Z				First Byte of next cell		

FIGURE 19

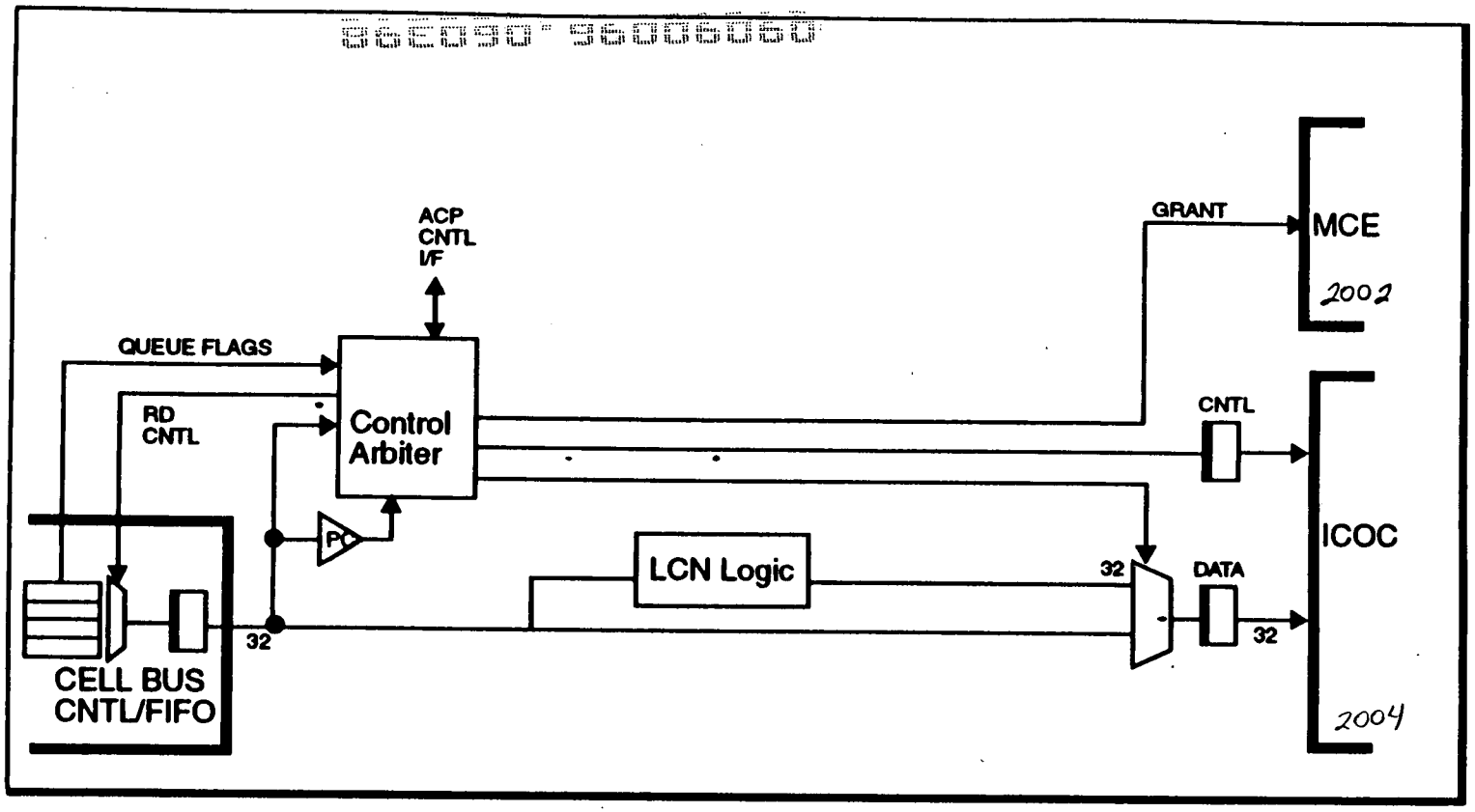
ACP
CNTL
I/F
GRANT
MCE
2002
QUEUE FLAGS
RD
CNTL
Control
Arbiter
CNTL
ICOC
PC
LCN Logic
32
DATA
32
32
CELL BUS
CNTL/FIFO
2004

FIGURE 20

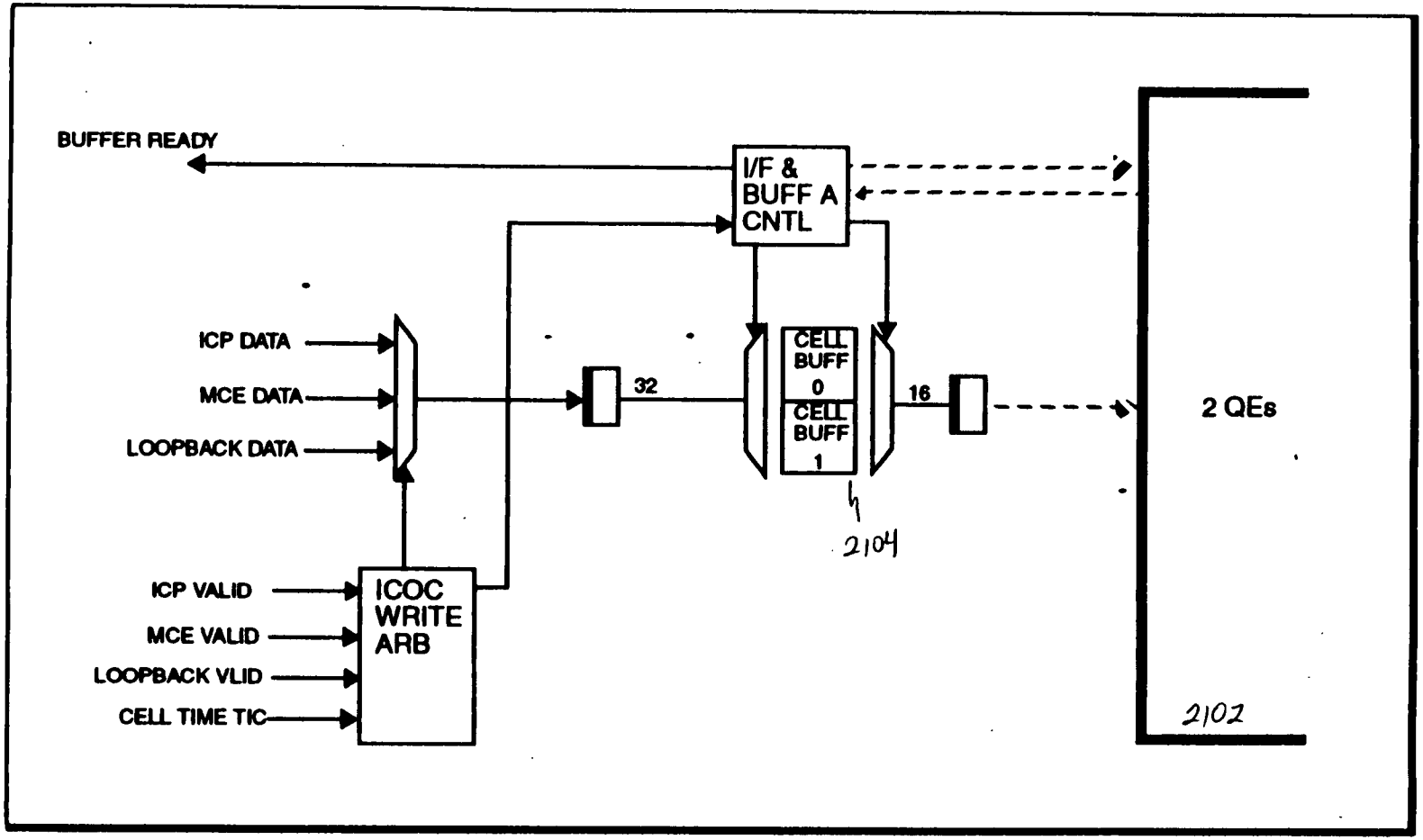
BUFFER READY
I/F & BUFF A CNTL
ICP DATA
MCE DATA
LOOPBACK DATA
32
CELL BUFF 0
CELL BUFF 1
16
2 QEs
2104
ICP VALID
MCE VALID
LOOPBACK VLID
CELL TIME TIC
ICOC WRITE ARB
2102

FIGURE 21

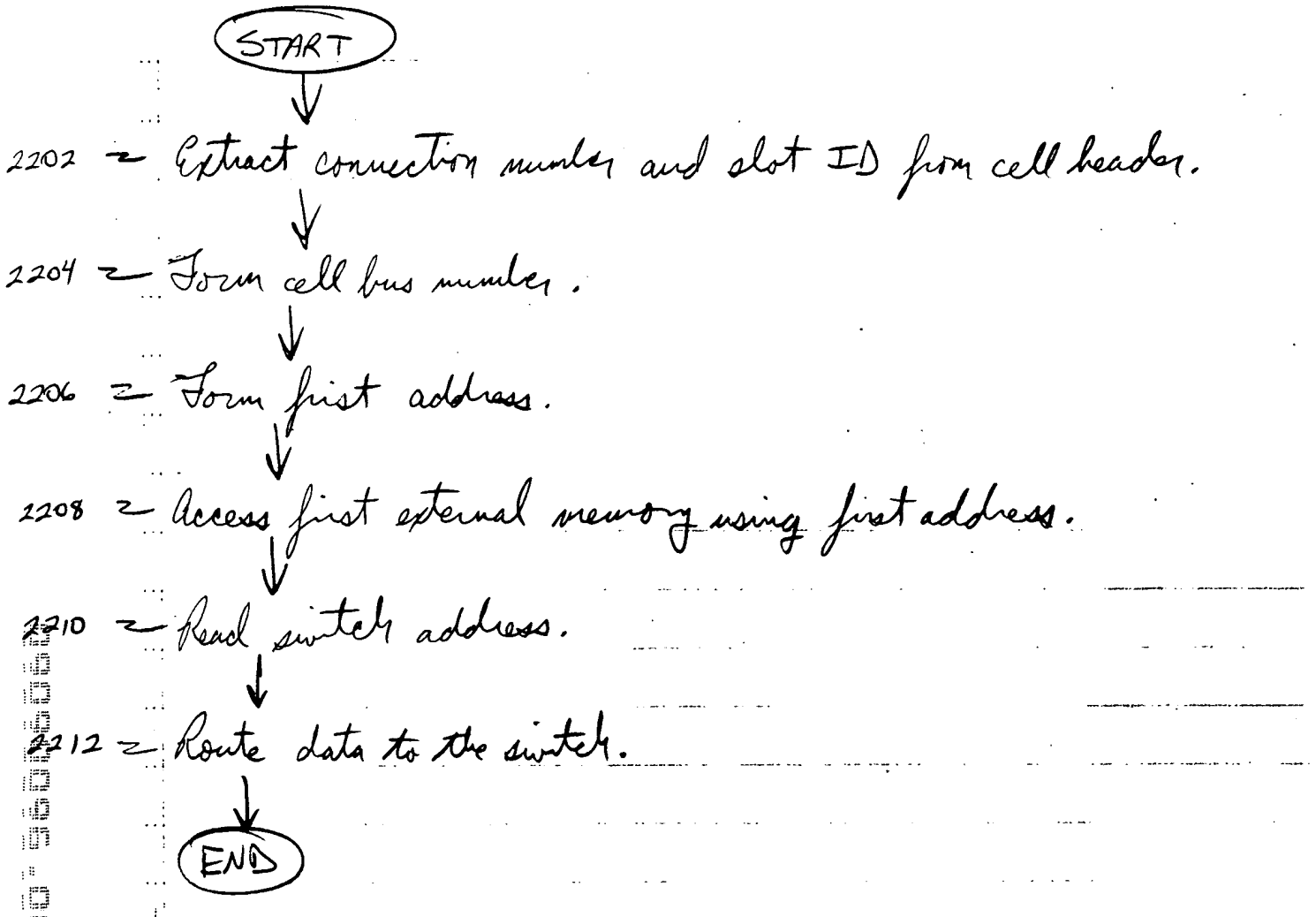
START
2202 – Extract connection number and slot ID from cell header.
2204 – Form cell bus number.
2206 – Form first address.
2208 – Access first external memory using first address.
2210 – Read switch address.
2212 – Route data to the switch.
END

FIGURE 22

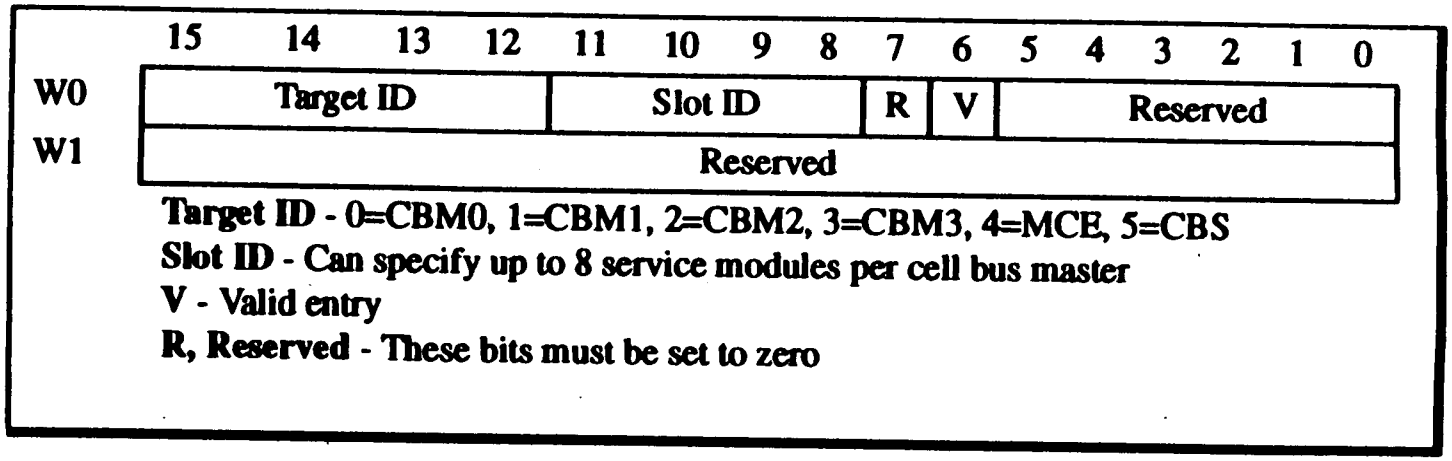
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
W0
W1
Target ID
Slot ID
R
V
Reserved
Reserved
Target ID - 0=CBM0, 1=CBM1, 2=CBM2, 3=CBM3, 4=MCE, 5=CBS
Slot ID - Can specify up to 8 service modules per cell bus master
V - Valid entry
R, Reserved - These bits must be set to zero

FIGURE 23

Firmware Information							CBC Hardware Information		
CBC Device Number	Device	Comment	Chassis Slot Number	Cell Bus Number	Physical Slot ID (on that Cell Bus)	QE Chip Number	CBC Chip Logic	QE Chip TX Address	Address Map RAM (Addressed by the QE TX Address)
0	SM0	Fast or Slow SM	1	0	1	0	CBM0	0	0x01
1	SM1	Fast or Slow SM	2	0	2	0	CBM0	1	0x02
2	SM2	Fast or Slow SM	3	1	3	0	CBM1	2	0x13
3	SM3	Fast or Slow SM	4	1	4	0	CBM1	3	0x14
4	SM4	Fast or Slow SM	5	2	5	0	CBM2	4	0x25
5	SM5	Fast or Slow SM	6	2	6	0	CBM2	5	0x26
6	SM6	Slow SM only	17	3	1	0	CBM3	6	0x31
7	SM7	Slow SM only	18	3	2	0	CBM3	7	0x32
8	SM8	Slow SM only	19	3	3	0	CBM3	8	0x33
9	SM9	Slow SM only	20	3	4	0	CBM3	9	0x34
10	SM10	Slow SM only	21	3	5	0	CBM3	10	0x35
11	SM11	Slow SM only	22	3	6	0	CBM3	11	0x36
12	MCE	Internal to CBC	N/A	N/A	N/A	0	MCE	12	0x40
13	Slave	Internal to CBC (RX is Connected to PSM in Slot 8, TX is NOT USED)	8 for PSM Card in Slot 7, 7 for PSM Card in Slot 8	N/A	N/A	0	CBS	13	NOT USED
14-15	Not Used	NOT USED	N/A	N/A	N/A	0	N/A	14-15	

FIGURE 24

*Firmware Information							CBC Hardware Information		
CBC Device Number	Device	Comment	Chassis Slot Number	Cell Bus Number	Physical Slot ID (on that Cell Bus)	QE Chip Number	CBC Chip Logic	QE Chip TX Address	Address Map RAM (Addressed by the QE TX Address)
16	SM0	Fast or Slow SM	9	4	9	1	CBM0	0	0x09
17	SM1	Fast or Slow SM	10	4	10	1	CBM0	1	0x0A
18	SM2	Fast or Slow SM	11	5	11	1	CBM1	2	0x1B
19	SM3	Fast or Slow SM	12	5	12	1	CBM1	3	0x1C
20	SM4	Fast or Slow SM	13	6	13	1	CBM2	4	0x2D
21	SM5	Fast or Slow SM	14	6	14	1	CBM2	5	0x2E
22	SM6	Slow SM only	25	7	9	1	CBM3	6	0x39
23	SM7	Slow SM only	26	7	10	1	CBM3	7	0x3A
24	SM8	Slow SM only	27	7	11	1	CBM3	8	0x3B
25	SM9	Slow SM only	28	7	12	1	CBM3	9	0x3C
26	SM10	Slow SM only	29	7	13	1	CBM3	10	0x3D
27	SM11	Slow SM only	30	7	14	1	CBM3	11	0x3E
28	MCE	Internal to CBC	N/A	N/A	N/A	1	MCE	12	0x40
29	Slave	Internal to CBC NOT USED	N/A	N/A	N/A	1	CBS	13	NOT USED
30-31	Not Used	NOT USED	N/A	N/A	N/A	1	N/A	14-15	NOT USED

FIGURE 25

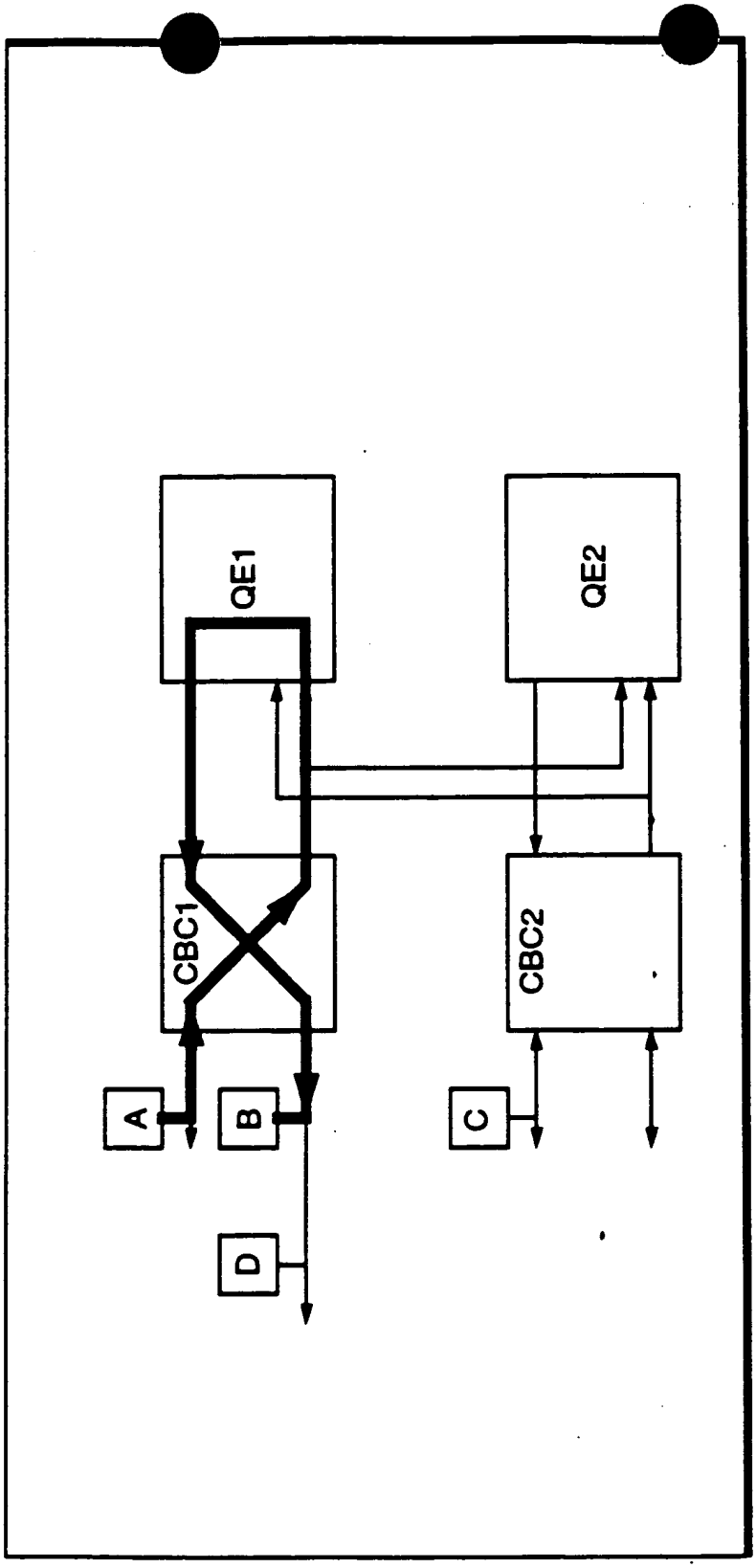

FIGURE 26

96C090 9606060

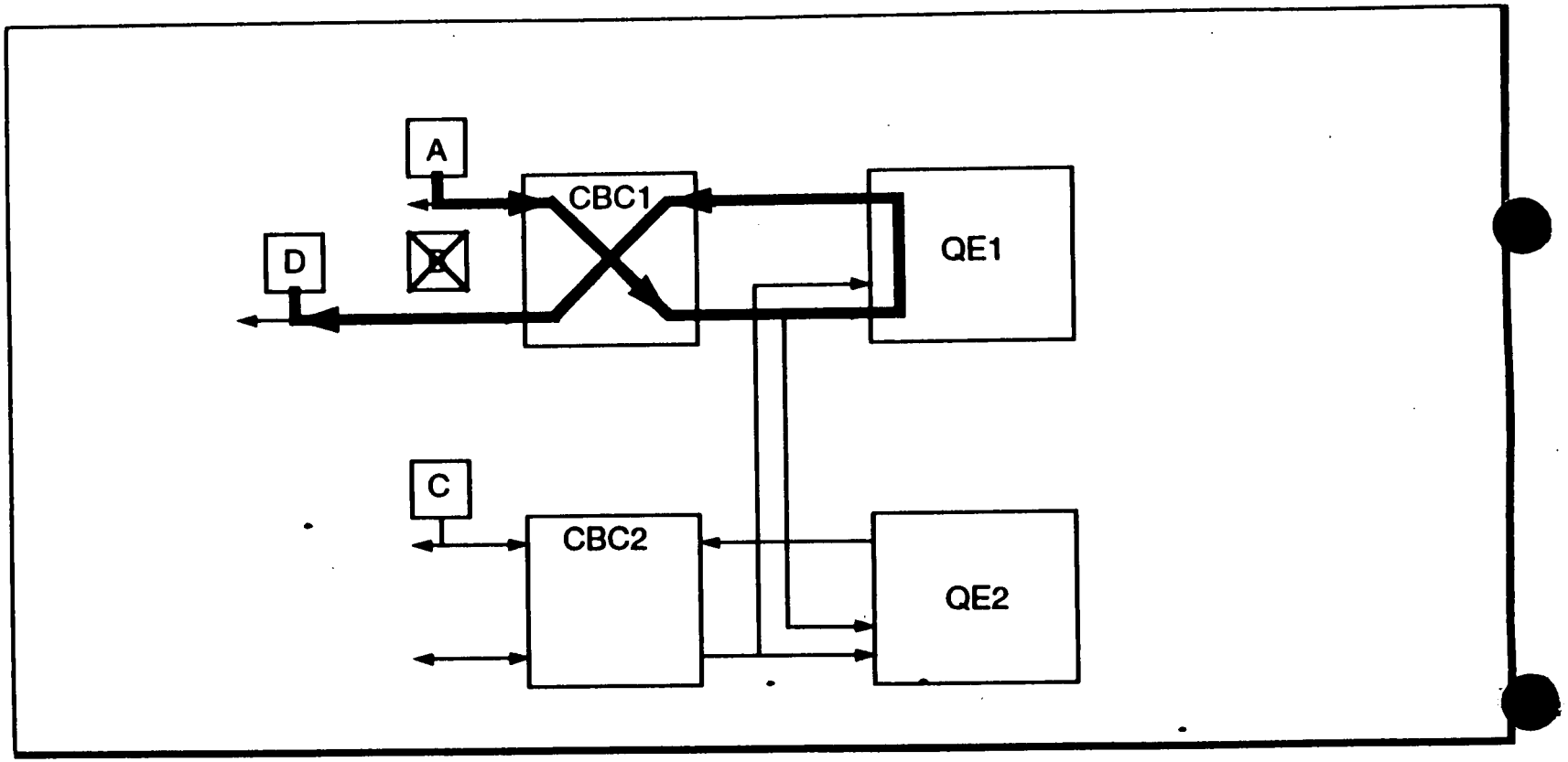

FIGURE 27

86C090 9606060

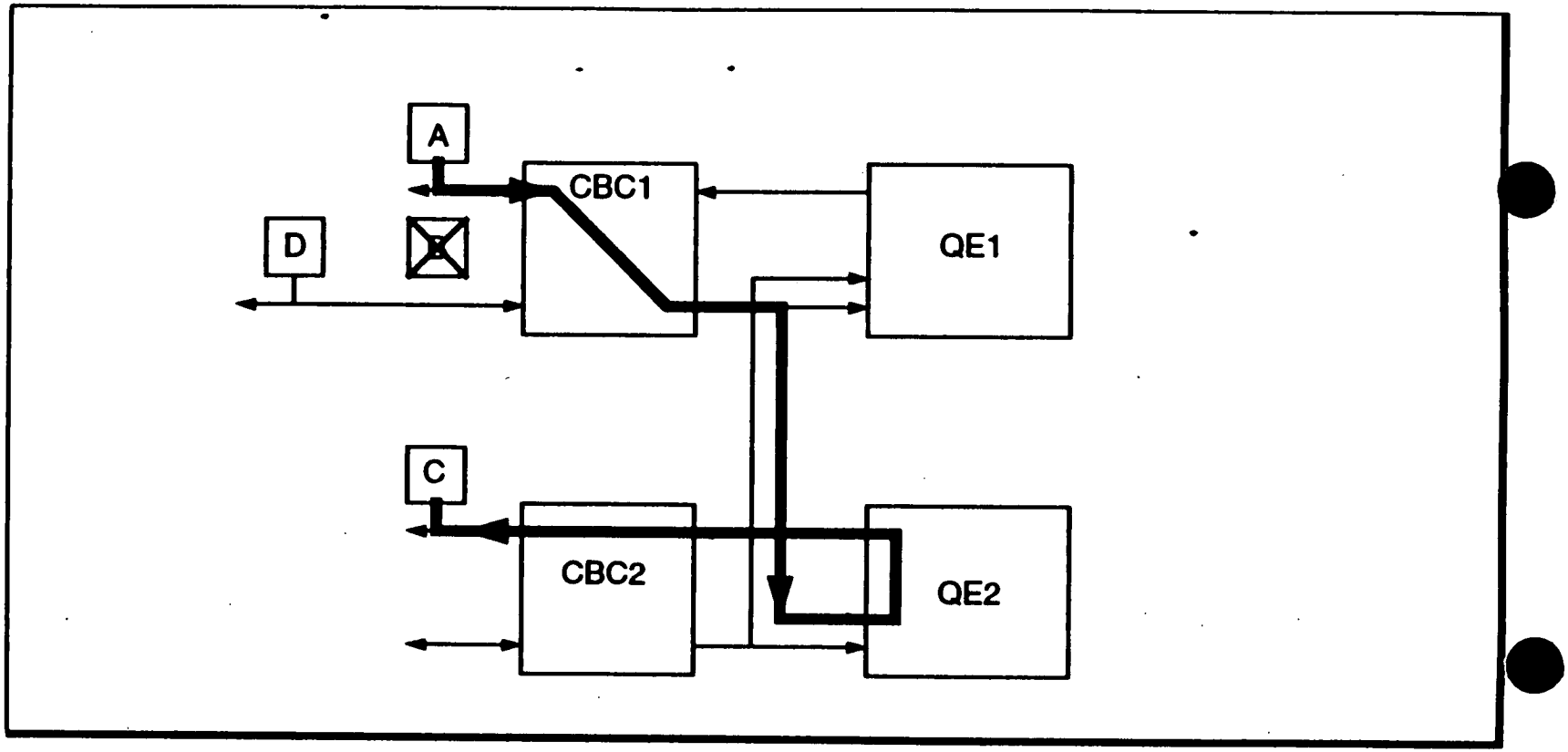

FIGURE 28

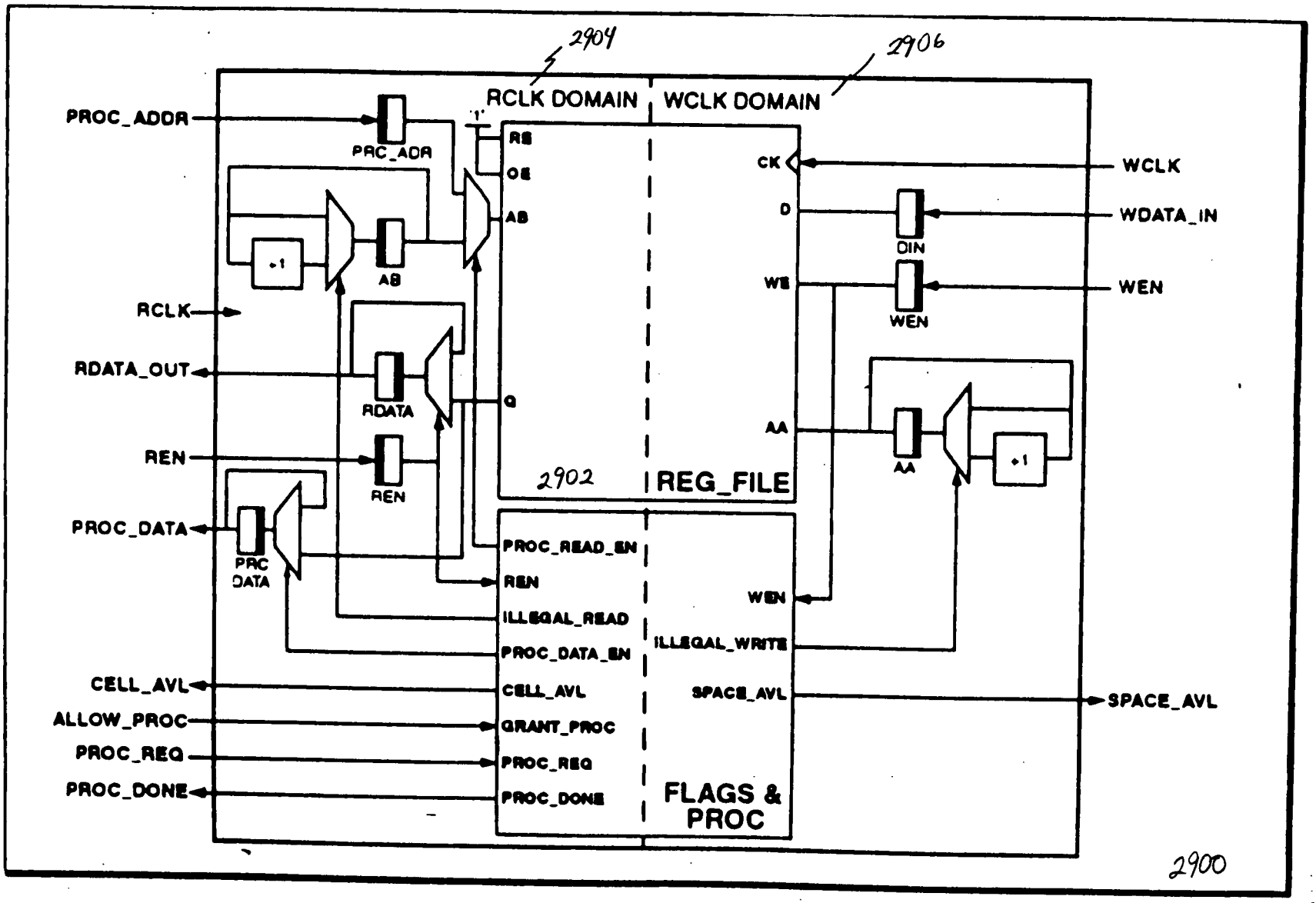
2904
2906
RCLK DOMAIN
WCLK DOMAIN
PROC_ADDR
PRC_ADR
'1'
RS
OE
AB
CK
WCLK
D
WDATA_IN
DIN
WE
WEN
WEN
+1
AB
RCLK
RDATA_OUT
RDATA
Q
AA
AA
+1
REN
REN
2902
REG_FILE
PROC_DATA
PRC DATA
PROC_READ_EN
REN
WEN
ILLEGAL_READ
ILLEGAL_WRITE
PROC_DATA_EN
CELL_AVL
CELL_AVL
SPACE_AVL
SPACE_AVL
ALLOW_PROC
GRANT_PROC
PROC_REQ
PROC_REQ
PROC_DONE
PROC_DONE
FLAGS &
PROC
2900

FIGURE 29

Parameter	Purpose	CBM Egress FIFO	CBM Ingress FIFO	CBS Ingress FIFO
num_bits_in_fifo_word	Number of bits in each FIFO word	34	34	34
num_words_in_cell	Number of words in one cell	14	14	14
log2_num_words_in_cell	Minimum bits needed to represent num_words_in_cell	4	4	4
num_cells_in_fifo	Number of cells in the FIFO	8	8	16
log2_num_cells_in_fifo	Minimum bits needed to represent num_cells_in_fifo	3	3	4
log2_num_words_in_fifo	Number of bits in FIFO address	7	7	8
wclk_2_rclk_ratio	WCLK to RCLK frequency ratio (minimum = 1) - WCLK=50 MHZ RCLK=21 MHZ RATIO=3 WCLK=21 MHZ RCLK =50 MHZ RATIO = 1	3	1	1
rclk_2_wclk_ratio	RCLK to WCLK frequency ratio (minimum = 1) - RCLK=50 MHZ WCLK=21 MHZ RATIO=3 RCLK=21 MHZ WCLK =50 MHZ RATIO = 1	1	3	3

FIGURE 30

Name	Count	Direction	Comments
Write Port Interface			
write_clk_i	1	Input	Write Port Clock
wclk_reset_i	1	Input	Write Port Reset
write_data_i	num_bits_in_fifo_word	Input	Write Data Input
write_en_i	1	Input	Write Enable
write_cell_cntr_o	log2_num_cells_in_fifo	Output	Write Port Cell Count
cell_space_avail_o	1	Output	Room for at least one more cell
Read Port Interface			
read_clk_i	1	Input	Read Port Clock
rclk_reset_i	1	Input	Read Port Reset
read_data_o	num_bits_in_fifo_word	Output	Read Data Output
read_en_i	1	Input	Read Enable
read_cell_cntr_o	log2_num_cells_in_fifo	Output	Read Port Cell Count
cell_avail_o	1	Output	At least one more cell in FIFO
allow_proc_read_i	1	Input	Granting Processor Port for reading; When the allow_proc_read_i is asserted, the Read Port is not allowed to read. In addition, the next 2 cycles following the last cycle the allow_proc_read_i is asserted are also not available.
Processor Port Interface			
proc_read_req_i	1	Input	Processor request read operation
proc_read_adrs_i	log2_num_words_in_fifo	Input	Processor read address
proc_read_data_o	num_bits_in_fifo_word	Output	Processor read data
proc_read_done_o	1	Output	Processor read request completed
BIST Interface			
bist_test_i	1	Input	
bist_cntl_i	1	Input	
bit_flag_o	1	Output	
bist_complete_o	1	Output	

FIGURE 31

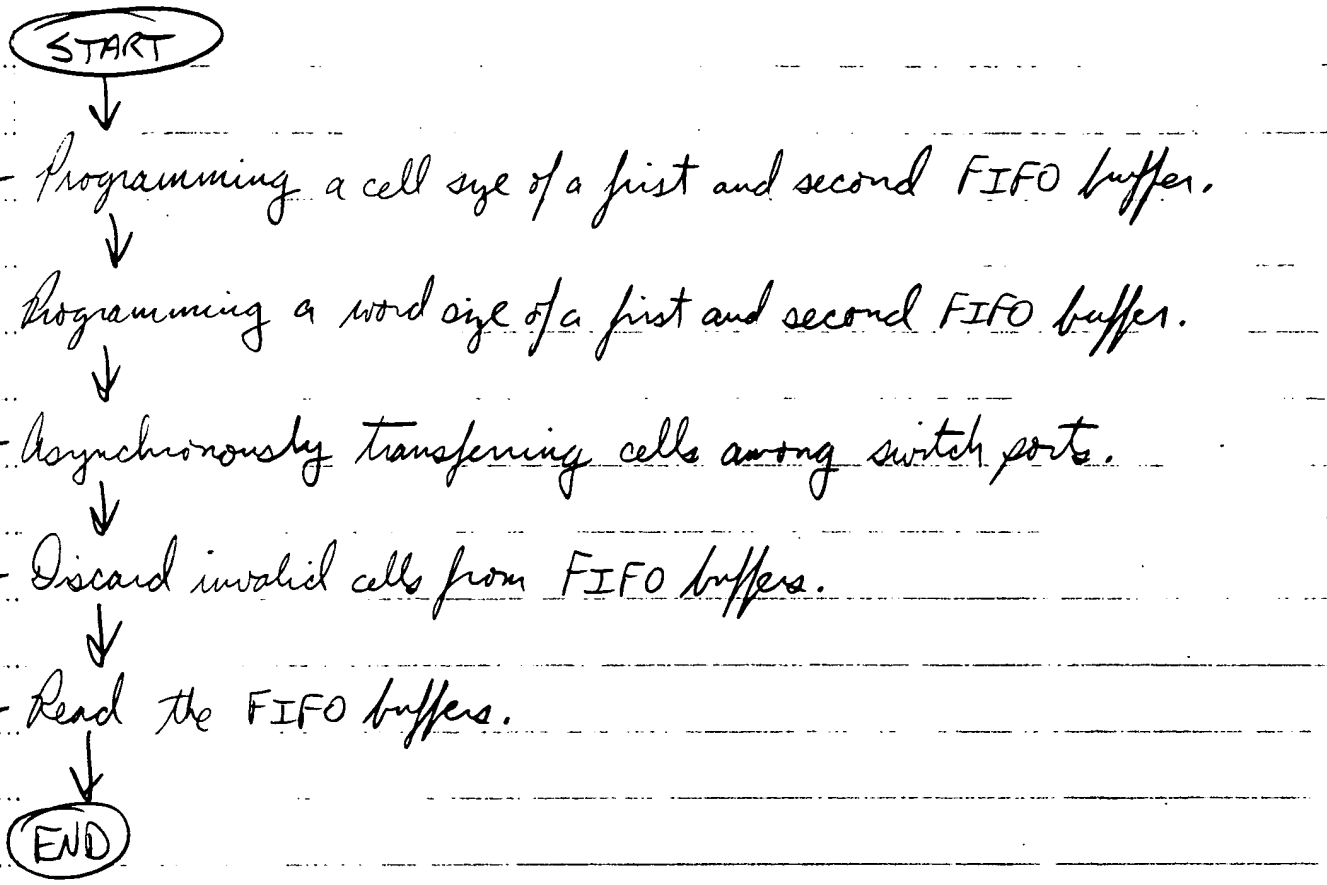
START
3202 – Programming a cell size of a first and second FIFO buffer.
3204 – Programming a word size of a first and second FIFO buffer.
3206 – Asynchronously transferring cells among switch ports.
3208 – Discard invalid cells from FIFO buffers.
3210 – Read the FIFO buffers.
END

FIGURE 32

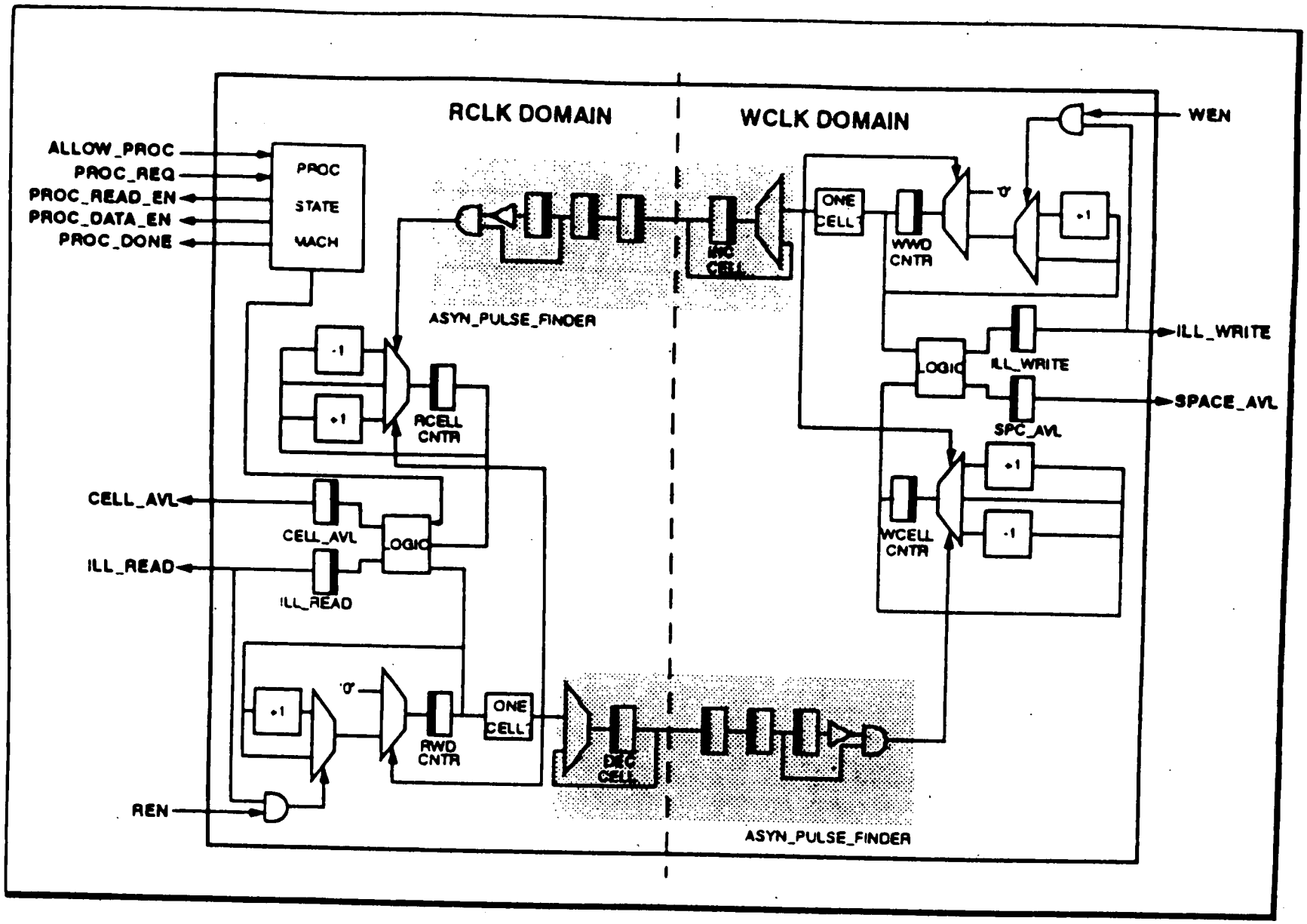
RCLK DOMAIN
WCLK DOMAIN
ALLOW_PROC
PROC_REQ
PROC_READ_EN
PROC_DATA_EN
PROC_DONE
PROC
STATE
MACH
WEN
ONE CELL
WWD CNTR
ASYN_PULSE_FINDER
ILL_WRITE
LOGIC
SPACE_AVL
SPC_AVL
RCELL CNTR
WCELL CNTR
CELL_AVL
ILL_READ
RWD CNTR
REN
ASYN_PULSE_FINDER

FIGURE 33

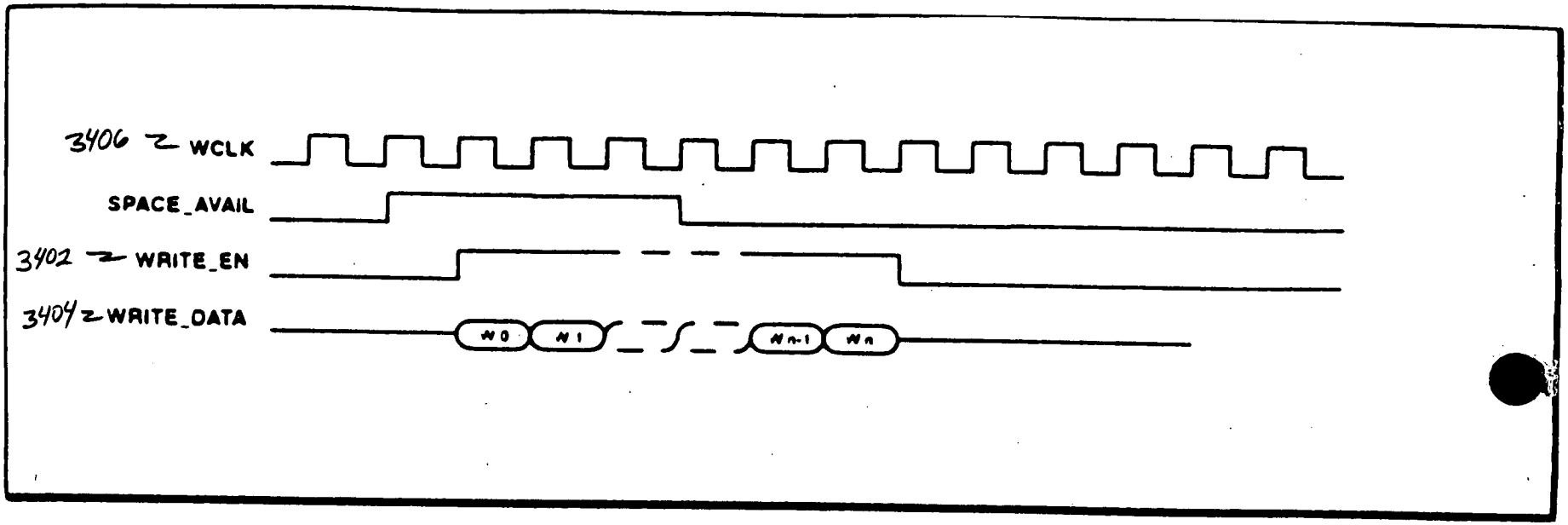
3406 WCLK
SPACE_AVAIL
3402 WRITE_EN
3404 WRITE_DATA
W0
W1
Wn-1
Wn

FIGURE 34

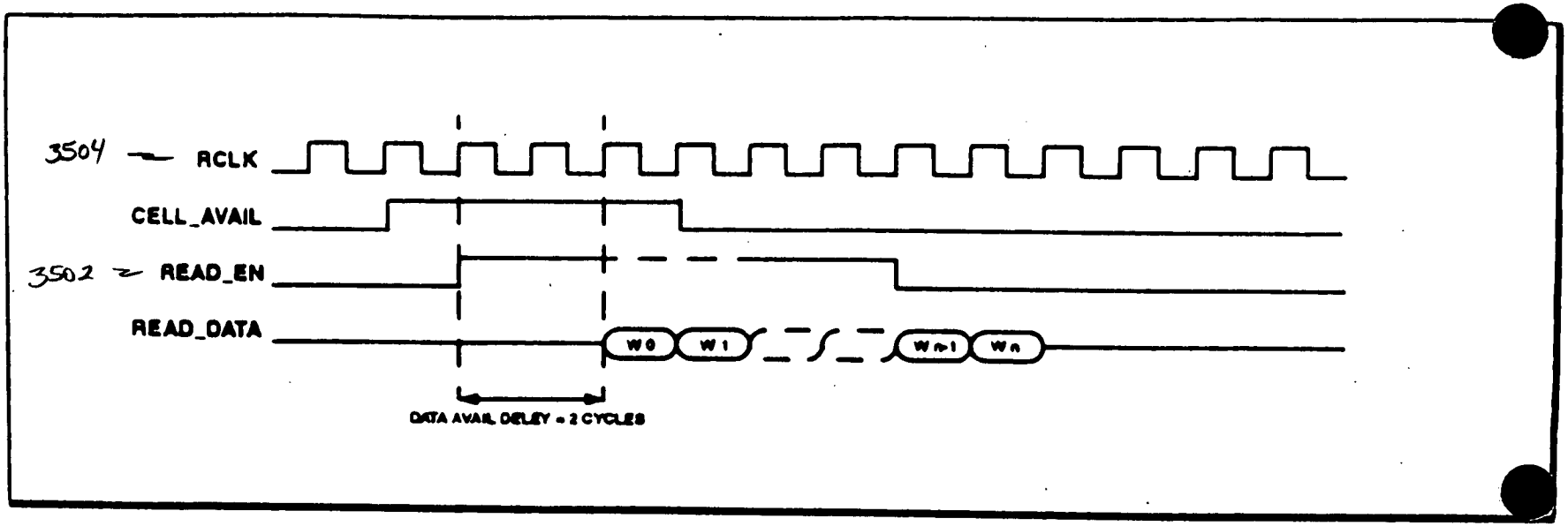
3504
RCLK
CELL_AVAIL
3502
READ_EN
READ_DATA
W0
W1
Wn-1
Wn
DATA AVAIL DELEY = 2 CYCLES

FIGURE 35

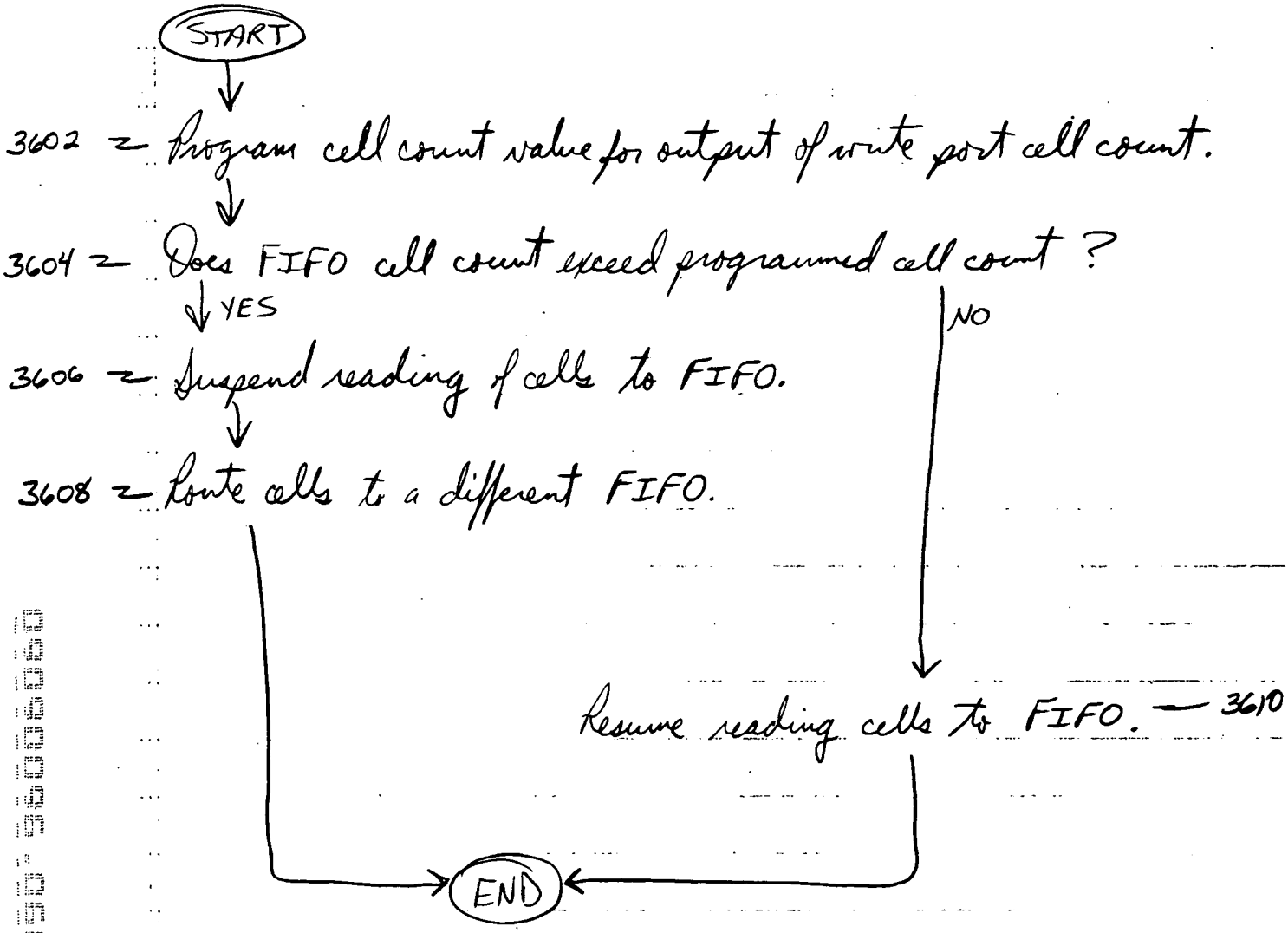
START
3602 – Program cell count value for output of route port cell count.
3604 – Does FIFO cell count exceed programmed cell count ?
YES
NO
3606 – Suspend reading of cells to FIFO.
3608 – Route cells to a different FIFO.
Resume reading cells to FIFO. – 3610
END

FIGURE 36

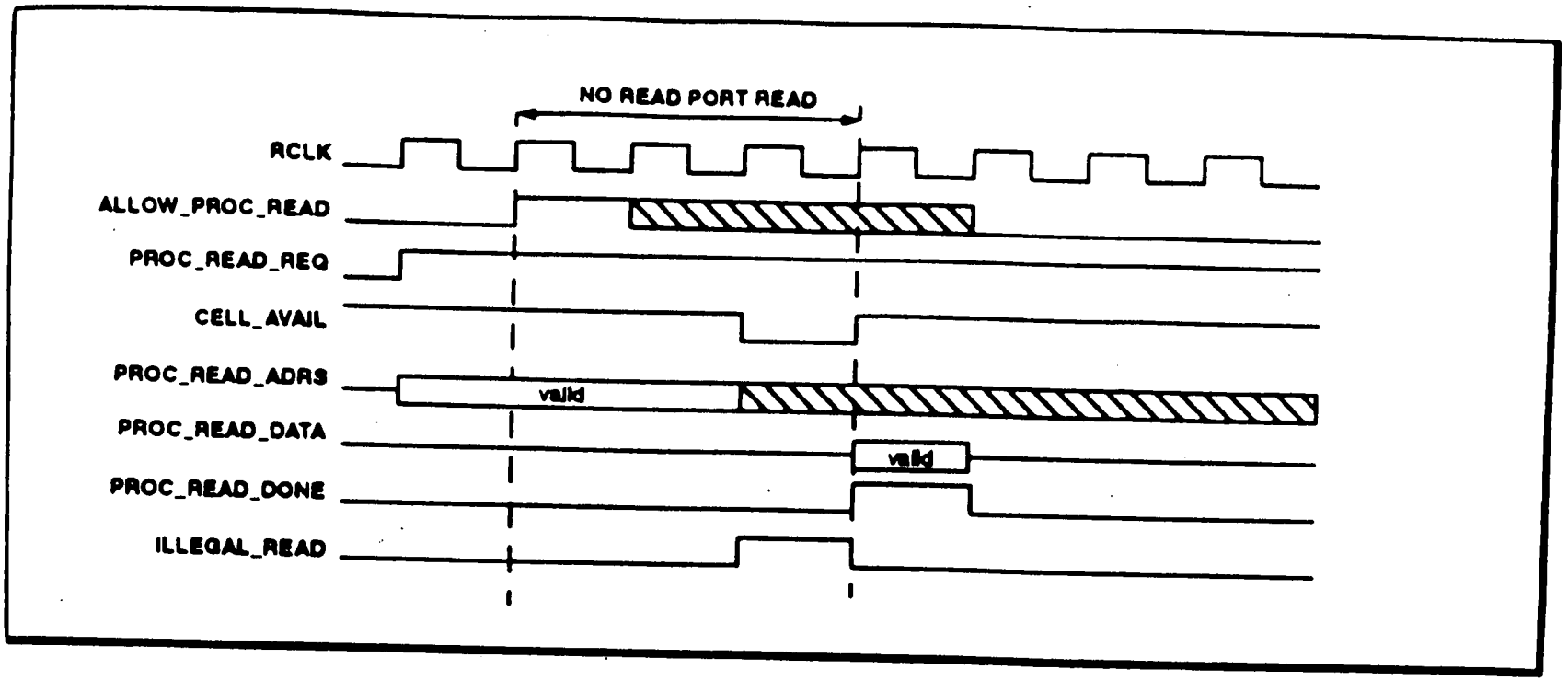
NO READ PORT READ
RCLK
ALLOW_PROC_READ
PROC_READ_REQ
CELL_AVAIL
PROC_READ_ADRS
valid
PROC_READ_DATA
valid
PROC_READ_DONE
ILLEGAL_READ

FIGURE 37

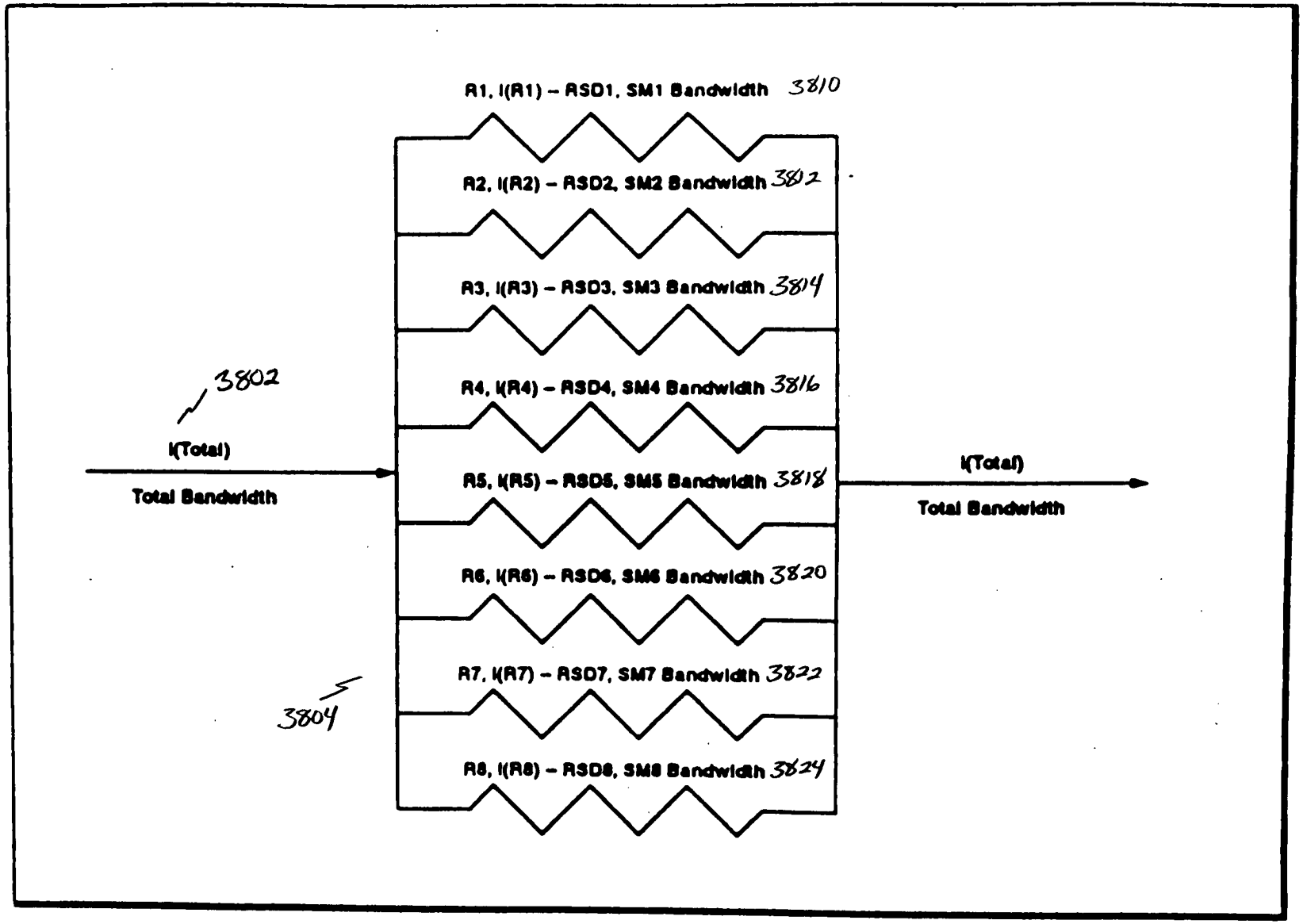
R1, I(R1) – RSD1, SM1 Bandwidth 3810
R2, I(R2) – RSD2, SM2 Bandwidth 3812
R3, I(R3) – RSD3, SM3 Bandwidth 3814
R4, I(R4) – RSD4, SM4 Bandwidth 3816
R5, I(R5) – RSD5, SM5 Bandwidth 3818
R6, I(R6) – RSD6, SM6 Bandwidth 3820
R7, I(R7) – RSD7, SM7 Bandwidth 3822
R8, I(R8) – RSD8, SM8 Bandwidth 3824
3802
I(Total)
Total Bandwidth
I(Total)
Total Bandwidth
3804

FIGURE 38

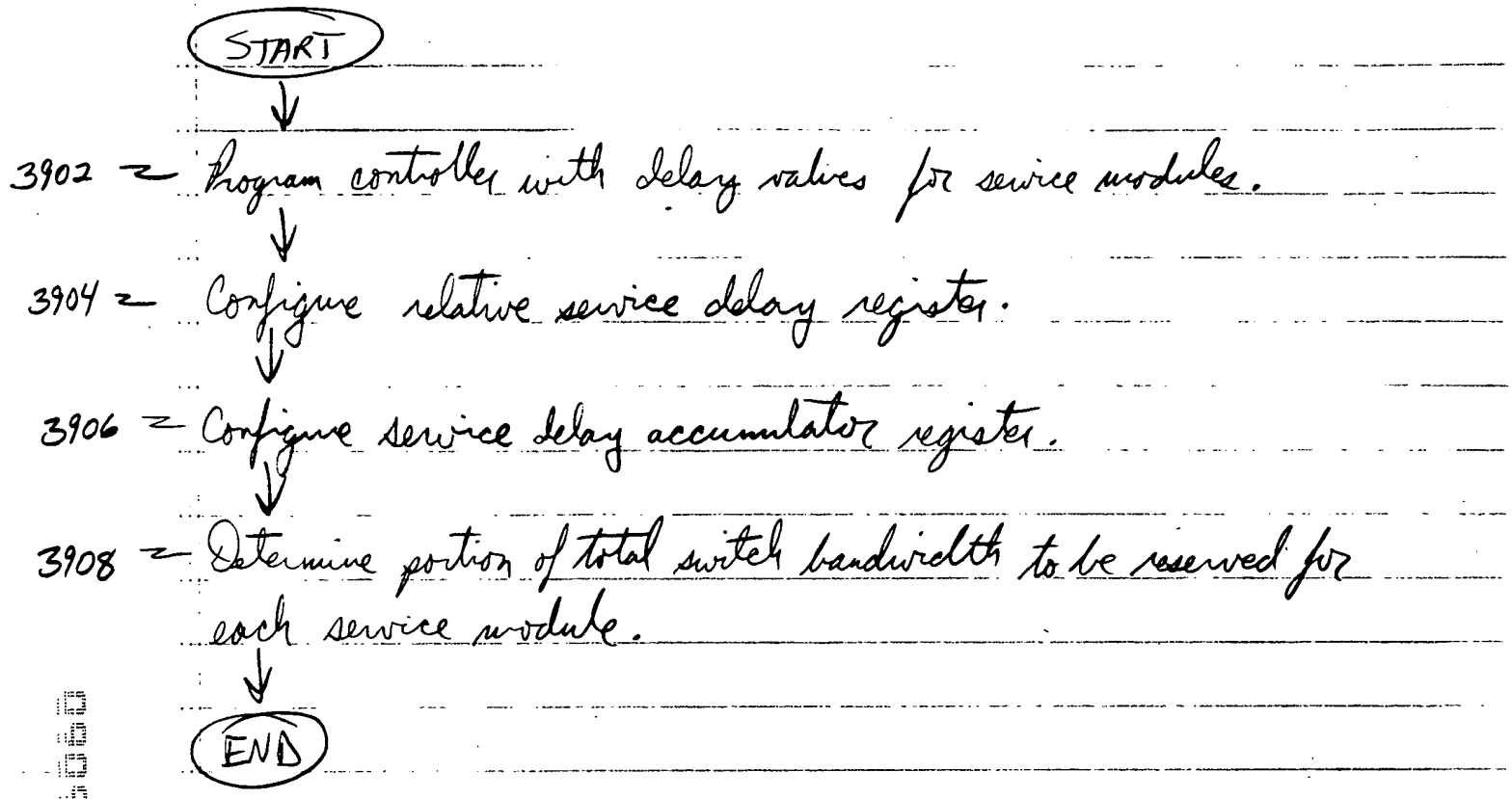
START
3902 – Program controller with delay values for service modules.
3904 – Configure relative service delay register.
3906 – Configure service delay accumulator register.
3908 – Determine portion of total switch bandwidth to be reserved for each service module.
END

FIGURE 39

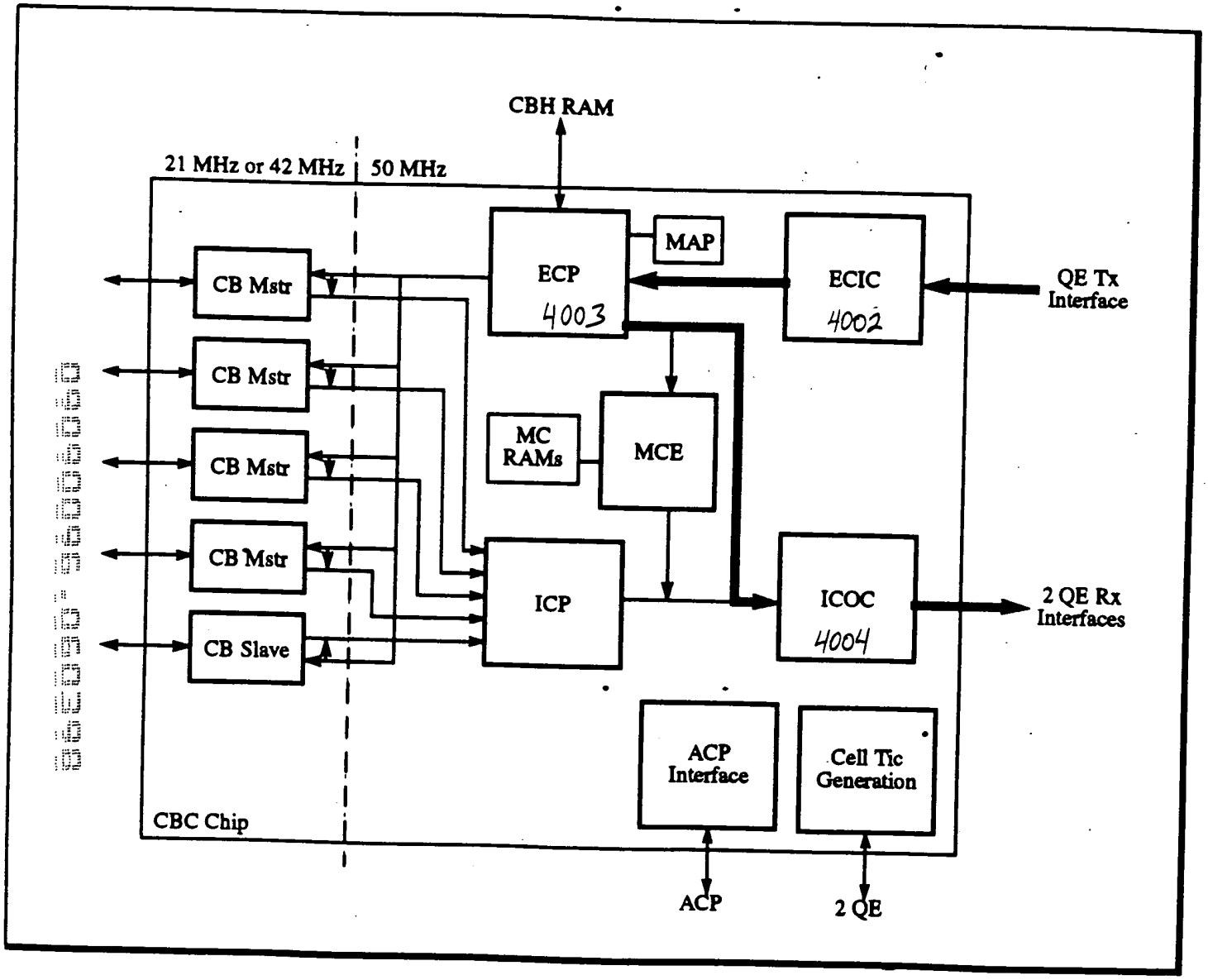
CBH RAM
21 MHz or 42 MHz
50 MHz
CB Mstr
CB Mstr
CB Mstr
CB Mstr
CB Slave
ECP
4003
MAP
ECIC
4002
QE Tx
Interface
MC
RAMs
MCE
ICP
ICOC
4004
2 QE Rx
Interfaces
ACP
Interface
Cell Tic
Generation
CBC Chip
ACP
2 QE

FIGURE 40

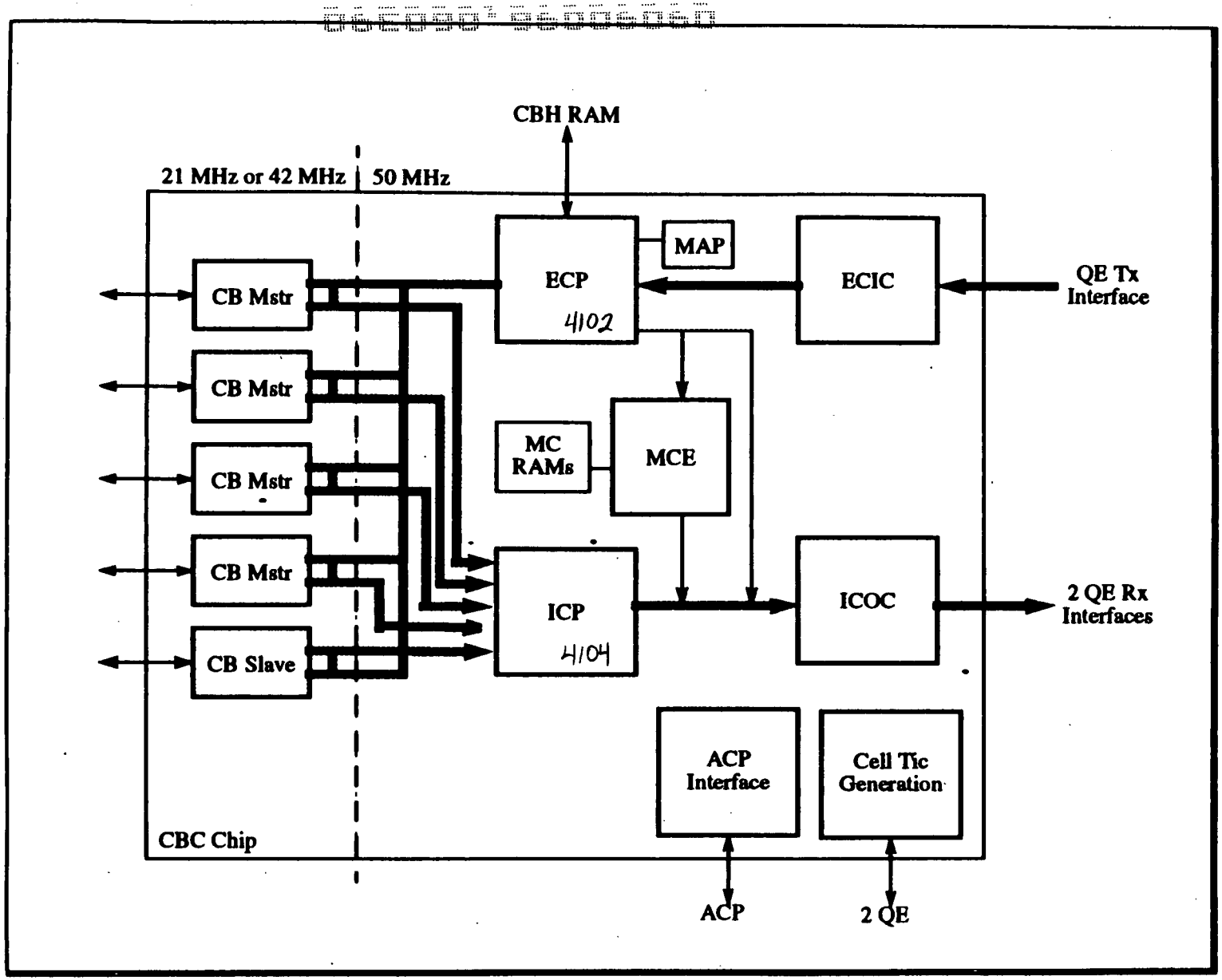
CBH RAM
21 MHz or 42 MHz
50 MHz
CB Mstr
CB Mstr
CB Mstr
CB Mstr
CB Slave
ECP
4102
MAP
ECIC
QE Tx Interface
MC RAMs
MCE
ICP
4104
ICOC
2 QE Rx Interfaces
ACP Interface
Cell Tic Generation
CBC Chip
ACP
2 QE

FIGURE 41